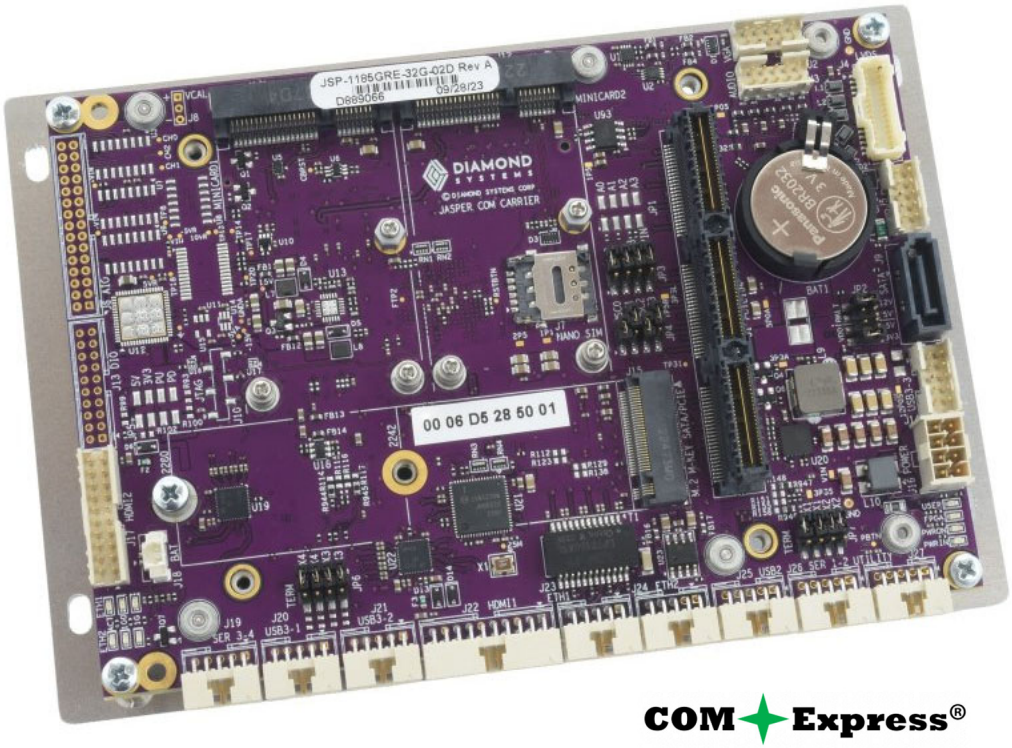
JASPER

COM-Based SBC with Integrated Data Acquisition

Featuring COM Express Type 6 Compact / Basic COMs

User Manual

Revision 2.2



Diamond Systems Corporation
Sunnyvale, CA 94086 USA

Technical Support Request Form
Tel: 1-650-810-2500
Revision 2.2

Contents

Notices
Technical Support Please use the Technical Support Request form to request assistance with a product you have already purchased.
Product and Sales Inquiry Please use the Sales Inquiry form to request assistance with selecting a product for your application, or to obtain further information about products and service.
Limited Warranty Diamond Systems Corporation provides a Limited Warranty for all items in this guide that it manufactures and sells, pursuant to terms provided in the Diamond Systems Corporation Limited Warranty. No other warranty, express or implied, is included. Please download the warranty for additional information.
Trademarks All trademarks, logos and brand names are the property of their respective owners.

Important Safe Handling Information

WARNING!

ESD-Sensitive Electronic Equipment

Observe ESD-safe handling procedures when working with this product.

Always use this product in a properly grounded work area and wear appropriate ESD-preventive clothing and/or accessories.

Always store this product in ESD-protective packaging when not in use.

Safe Handling Precautions

The Osbourne carrier board contains a high number of I/O connectors with connections to sensitive electronic components. This creates many opportunities for accidental damage during handling, installation, and connection to other equipment.

This section provides critical, best practice suggestions to avoid damage to your products. It includes descriptions of many common causes of damage – all of which can void your warranty.

Please follow these guidelines to be aware of common causes of damage and take the necessary precautions to prevent damage to your Diamond Systems' (or any vendor's) embedded computer boards.

Damage from incorrect handling or storage

- Physical and electronic damage can occur from mishandling. The following are frequent scenarios.
- An electrostatic discharge (ESD) causes a board to malfunction or stop working entirely. If ESD occurs, typically there is no visual sign of damage. While it is often difficult to identify faulty component(s), if the fault is identified there is a good chance that the board can be repaired.
- A screwdriver slips during installation, causing a gouge in the PCB surface and cutting signal traces or damaging components.
- A board is dropped, causing damage to the circuitry near the point of impact. Most of our boards are designed with at least 25 mils clearance between the board edge and any component pad, and ground / power planes are at least 20 mils from the edge. These design rules can minimize but cannot always prevent damage from impact.
- A short occurs when a metal screwdriver tip slips, or a screw drops onto a board while it is powered on. This can cause overvoltage or power supply problems described below.
- A storage rack with slots to hold boards can damage components near the board edge. Many boards have components that are close to the board edge, which are subject to damage in racks.
- Connector pins are bent by improperly dis-assembling attached boards or ribbon cables from a pin header, or from physical impact or improper storage. Typically, bent pins can be repaired one at a time with needle-nose pliers. Severely bent or frequently repaired pins may require the replacement of the connector.

Best Practices to avoid damage during handling or storage

- To prevent ESD damage, always follow proper ESD-prevention practices when handling any electronic components.
- To prevent physical damage from impact, handle all boards with care and work in a safe, spacious environment.
- To prevent short circuit damage from a metallic tool or dropped screw, perform assembly operations ONLY when the system is powered off.

- To prevent damage to fragile components and connector pins in storage, always store boards in individual ESD-safe sleeves in sturdy bins with dividers between boards. Do NOT use racks with slots, or stack boards in a pile or in close proximity.
- To prevent damage to connector pins during assembly or dis-assembly, use caution to align connectors and especially when force is needed to disassemble components and wires. Do not 'rock' connectors back and forth or pull any component at the wrong angle.

Damage due to incorrect voltage or connections

Power supply wired backwards

Diamond Systems power supplies and boards are not designed to withstand a reverse power supply connection. Reverse power will destroy nearly every IC that is connected to the power supply. Reverse power damage is rarely repairable. Check twice before applying power!

Board not installed properly in PC/104 stack

If a PC/104 board is accidentally shifted by 1 row or 1 column (of pins) it is possible for power and ground signals on the bus to contact the wrong pins. For example, this can damage components attached to the data bus because it puts the ±12V power supply lines directly on data bus lines.

Overvoltage on analog input

If a voltage applied to an analog input exceeds the design specification of the board, the input multiplexor and/or parts behind it can be damaged. Most of our boards will withstand an erroneous connection of up to ±35V on the analog inputs, even when the board is powered off, but not all boards, and not in all conditions.

Overvoltage on analog output

If an analog output is accidentally connected to another output signal or a power supply voltage, the output can be damaged. On most of our boards, a short circuit to ground on an analog output will not cause trouble.

Overvoltage on digital I/O line

If a digital I/O signal is connected to a voltage above the maximum specified voltage, the digital circuitry can be damaged. On most of our boards the acceptable range of voltages connected to digital I/O signals is 0-5V, and they can withstand about 0.5V beyond that (-0.5 to 5.5V) before being damaged. However, logic signals at 12V and even 24V are common, and if one of these is connected to a 5V logic chip, the chip will be damaged, and damage may extend past that chip to others in the circuit.

Best Practices to avoid damage due to incorrect voltage or connections

- Ensure all power supply connections are correct and not reversed!
- Ensure all pins are aligned properly before and after assembling boards and components!
- Ensure proper voltage is supplied to all analog inputs!
- Ensure all analog voltage outputs do not connect to another signal output or power supply output!
- Ensure all voltages for digital I/O lines are proper and with range, and that higher voltage signals (24V or 12V) are not supplied to lower voltage circuits (12V or 5V)!

IMPORTANT! Always check twice before Powering Up!

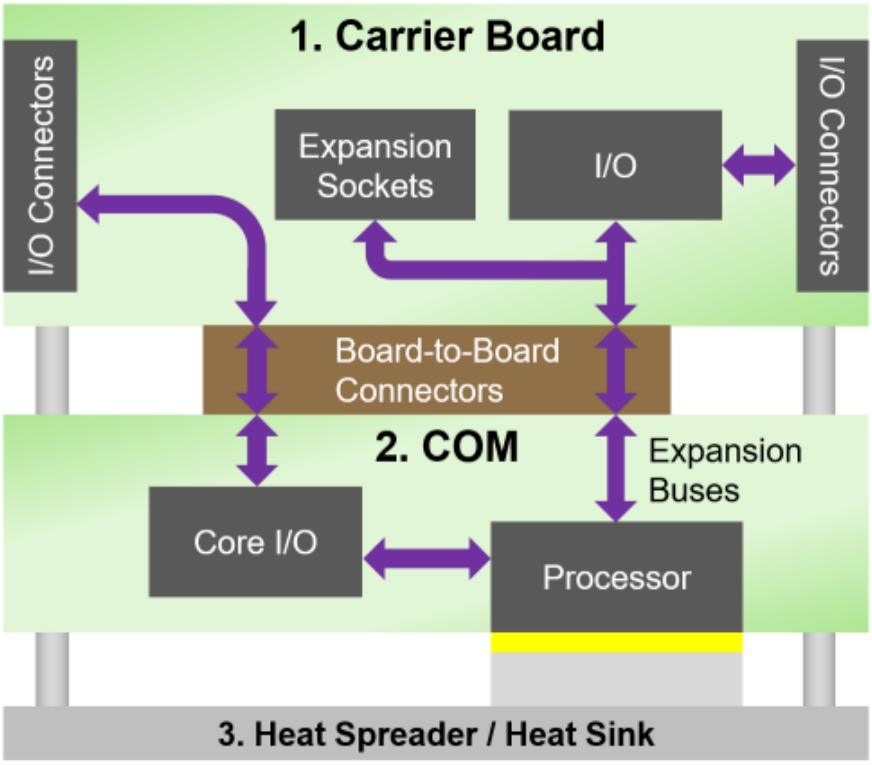
1. Introduction

1.1. Jasper Product Overview

Jasper is a compact rugged single-board computer (SBC) utilizing a COM Express module to provide performance scalability, extended product lifetime, and a reduced footprint due to a stacked board configuration. The SBC is available with a choice of COMs that have been tested for compatibility, offering a range of Core i7 and Xeon processors from both 11th and 13th generation families.

The use of a COM-based architecture yields many significant benefits over a true single-board computer where the processor and related circuitry are included on the main board:

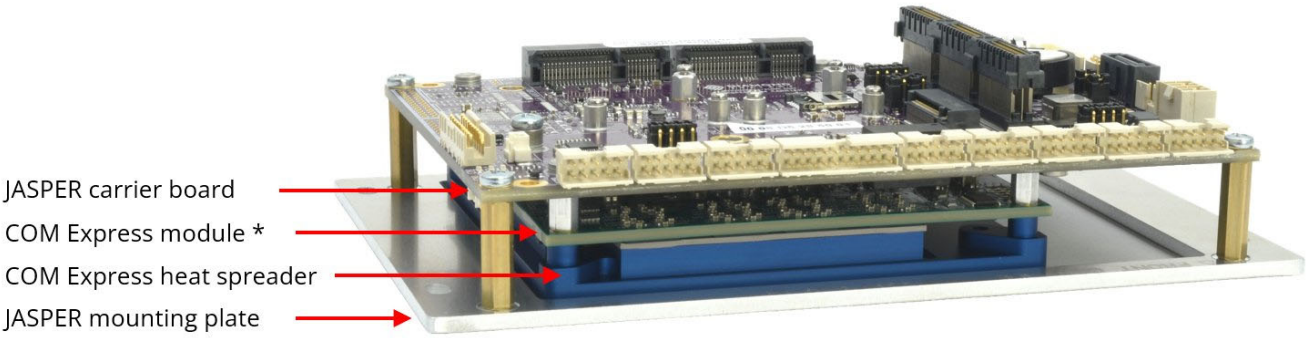
- **Scalable CPU performance -** you can swap out one COM for another in the exact same form factor but with a different CPU. This allows your system to be easily upgraded when software demands increase, while avoiding any mechanical redesign.
- **Extended product lifetime -** if the COM you're using becomes obsolete, another one can be used in its place easily, with no mechanical changes required to the system. This enables COM-based embedded systems to easily last 20 years, since most of the baseboard electronics usually have much longer lifecycles than the processor and related peripherals contained on the COM.
- **Higher feature density / smaller overall size -** the stacked 2-board design means you get more features per unit area in your system.
- **Earlier access to the latest CPU technology -** Most new processors are introduced in COMs long before they are available in true single-board computer form. With a COM-based SBC you can upgrade your system with the latest CPU sooner, again without having to engage in any mechanical redesign.
- **Consistent platform across product lines -** the CPU scalability and interchangeability mean that a single physical form factor can be used in multiple applications requiring different CPU capability.



Jasper is available with an integrated professional-quality data acquisition circuit featuring analog and digital I/O with full programming library support. It includes a wide range of built-in standard PC I/O plus expansion sockets for minicards and PCIe/104 I/O modules, making it a great choice for applications requiring any combination of high performance,

The COM Express module mounts on the bottom side of the board, and the PCIe104 expansion sockets are on the top side. The board dimensions are 4.000" x 5.750", matching the 3.5-inch form factor in size and mounting hole pattern.

A thicker PCB (.090" / 2.3mm), latching I/O connectors, and full -40/+85C operating temperature provide increased ruggedness, enabling the board to work reliably in mobile and harsh environment applications. Jasper is used as the processor in Diamond's rugged SabreCom and Geode rugged computer systems. The Jasper SBC has passed MIL-STD-202H shock and vibration testing, and the Geode system with Jasper SBC inside has passed MIL-STD-810H testing. Test reports are available on the product's web page.



* Jasper supports both Basic 95x125mm and Compact 95x95mm COM Express modules.

1.2. Processor Options

Jasper is available with a variety of installed COM Express modules. These COMs are all tested and approved by Diamond and have board support packages (configured operating system images) available for Windows 10 / 11 and Linux. The list of available processors may change from time to time as new COMs are tested and qualified. The table below lists the available options as of the publication date of this manual.

In many cases a COM not listed here may also work properly with minimal or no BIOS customization. However, COM vendors may implement various features in different configurations or quantities (especially the number and type of PCIe lanes), so certain features may not function if the COM doesn't provide the necessary interface for them. Please check with Diamond technical support if you are interested in using Jasper with a COM not listed here.

Generation	Type	Processor	PassMark* (approx.)	Max RAM
11 Tiger Lake	Core i7	1185GRE	8,000	32GB
11 Tiger Lake	Core i7	1185G7E	10,300	64GB
13 Raptor Lake	Core i7	1365URE	10,300	64GB
11 Tiger Lake	Xeon	11865MRE	19,600	96GB or ECC 32GB

(PassMark ratings are as reported by PassMark.com and are provided for comparison purposes only.)

1.3. Baseboard Variants

The baseboard used in Jasper is available in multiple configurations. Models BB02D and BB03A are normally in stock, while the lower cost BB01D normally requires a minimum order quantity.

Feature	Baseline JSP-BB01D	Full-Feature JSP-BB02D	Full Feature w/ DAQ JSP-BB03A
Availability	Special order	Stocked	Stocked
Gigabit Ethernet	1	2	2
Minicard socket	2	2	2
M.2 socket	1	1	1
SATA connector	1	1	1
HDMI	2	2	2
VGA*	1	1	1
LVDS	1	1	1
USB 3.0	3	3	3
USB 2.0	2	2	2
Serial Ports	2x RS-232	4x RS-232/422/485 (Jumper for protocol selection)	4x RS-232/422/485 (Jumper for protocol selection)
PCIe104 socket	No	Yes	Yes
Audio	No	1	1
Analog/Digital IO	No	No	16 SI/8 DE Ain 4 Aout 22 DIO
Others	4 GPI, 4 GPO I2C Reset & Power Button	4 GPI, 4 GPO I2C,1x RS232 Reset & Power Button	4 GPI, 4 GPO I2C, 1x RS232 Reset & Power Button

*Based on availability on the installed COM Express module

1.4. Jasper Ordering Guide

The table below lists the available standard configurations for the carrier board. This list is valid as of the publication date of this manual. As the board can work with multiple COMs, new COMs are tested and added regularly, so check the Diamond website or contact our sales department for currently available product models.

In general, when a new COM is added, OS support will also be available for the current versions of Windows and Ubuntu Linux.

Carrier board

JSP-BB01D	Jasper COM Carrier, low-cost model, 12V or 15-36VDC In (special order item)
JSP-BB02D	Jasper COM Carrier, PCIe/104 expansion, Digital I/O, 12V or 15-36VDC In
JSP-BB03A	Jasper COM Carrier, PCIe/104 and Data Acquisition, 12V or 15-36VDC In

Jasper SBC product (carrier board with installed COM and heat spreader; no OS installed)

JSP-1185G7E-64G-02D	JSP-BB02D with Intel 11th Gen Core i7, 64GB RAM, Heat Spreader
JSP-1185G7E-64G-03A	JSP-BB03A with Intel 11th Gen Core i7, 64GB RAM, Heat Spreader
JSP-1185GRE-32G-02D	JSP-BB02D with Intel 11th Gen Core i7-1185GRE, 32GB RAM Soldered, Heat Spreader
JSP-1365URE-64G-02D	JSP-BB02D with Intel 13th Gen Core i7-1365URE, 64GB RAM Soldered, Heat Spreader

Software development kits (Pre-configured OS on a flashdisk with backup USB memory stick)

SDK-JSP-1185G7E-LNX64	Linux 64-bit Software Development Kit for Jasper SBC with 11th Gen Core i7 (Inclusive of OS, Instruction for flashing, USB2.0 8GB Flash drive, M.2 2242 SATA 64GB wide temperature flash disk)
SDK-JSP-1185G7E-WE1064	Windows 10 64-bit Software Development Kit for Jasper SBC with 11th Gen Core i7 (Inclusive of OS, Instruction for flashing, USB2.0 8GB Flash drive, M.2 2242 SATA 64GB wide temperature flash disk)
SDK-JSP-1185GRE-LNX64	Linux 64-bit Software Development Kit for Jasper SBC with 1185GRE processor (Inclusive of OS, Instruction for flashing, USB2.0 8GB Flash drive, M.2 2242 SATA 64GB wide temperature flash disk)
SDK-JSP-1185GRE-WE1064	Windows 10 64-bit Software Development Kit for Jasper SBC with 1185GRE processor (Inclusive of OS, Instruction for flashing, USB2.0 8GB Flash drive, M.2 2242 SATA 64GB wide temperature flash disk)

Development kits (SBC + software development kit + cable kit)

DK-JSP-1185G7E-LNX64	Development Kit: Jasper 11th Gen Core i7 SBC with DIO, 64GB RAM, Linux 64-bit OS
DK-JSP-1185G7E-WE1064	Development Kit, Jasper SBC, 1185G7E CPU, Windows 10 64-Bit OS

Cable kit

CK-JSP-01	Jasper cable kit, full kit with data acquisition cables (for “A” models)
CK-JSP-02	Jasper cable kit, without data acquisition cables (for “D” models)

1.5. Product Photos

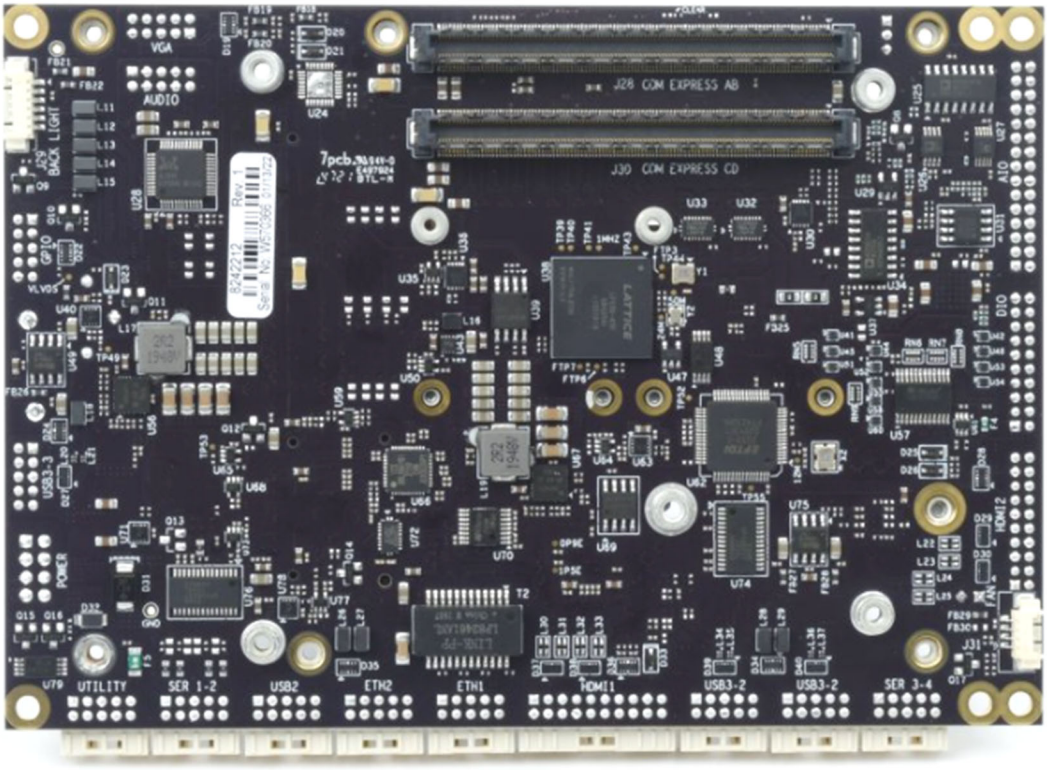


Figure 1-1: COM module installation side

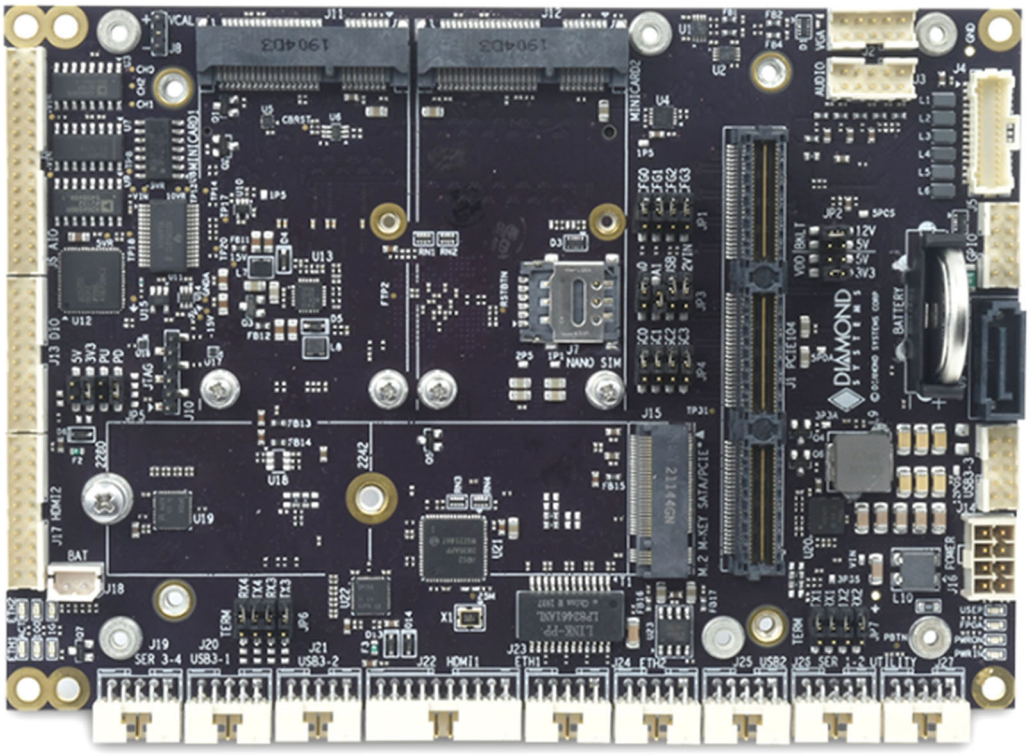


Figure 1-2: I/O expansion side ("A" model with data acquisition shown)

2. Feature List

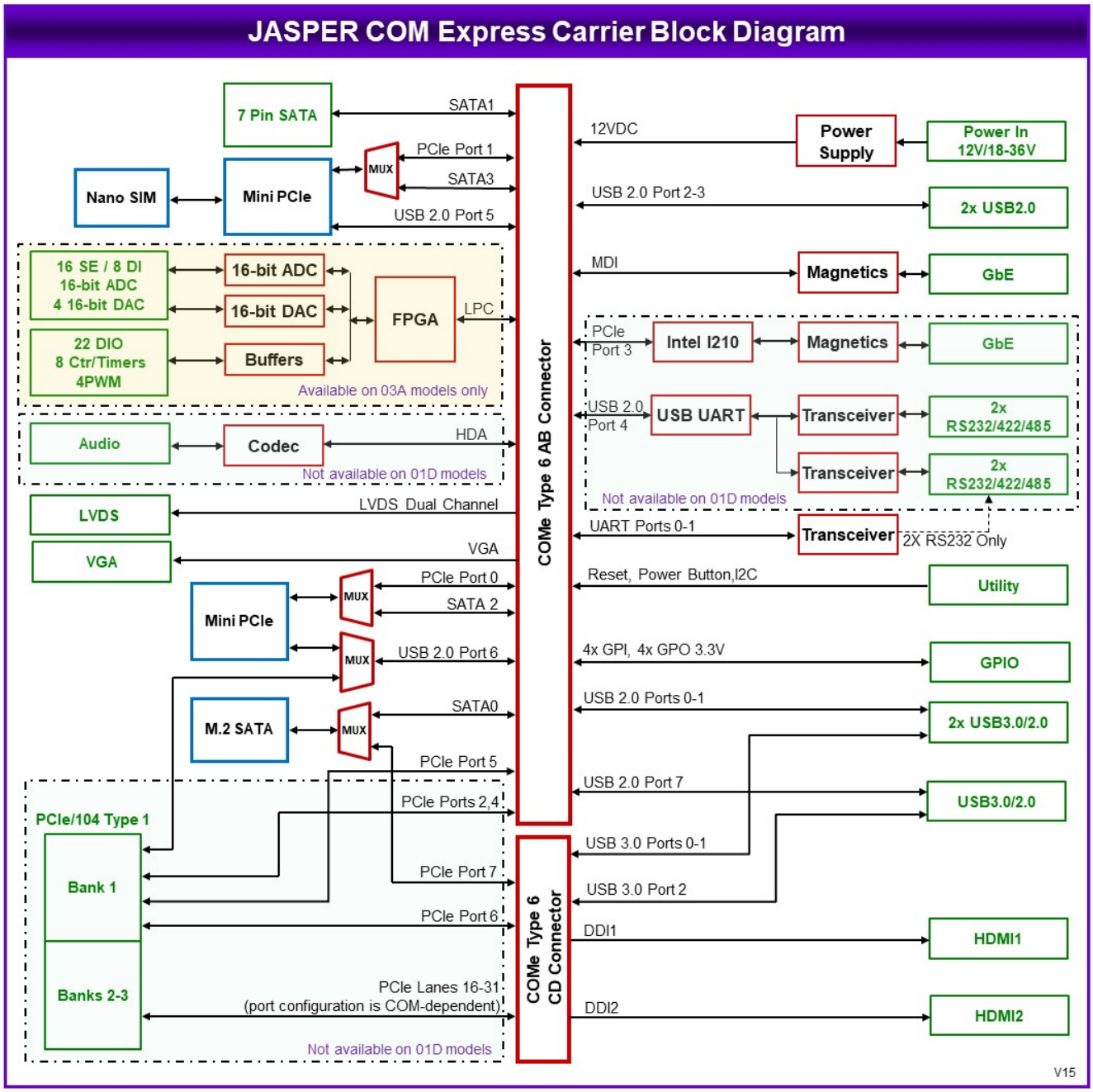
Feature	Description	Connector Type
Power	15V-36V wide input or 12V fixed supply (Selected using Jumper configuration at JP3)	8 Position Vertical Connector Header (J16)
RTC	3V power input for RTC functionality	On board battery 2032 holder Or 2 Position Vertical Connector Header (J18)
Ethernet	ETH-1 10/100/1000Mbps from COM module	10 Position RA Connector Header (J23)
	ETH-2 10/100/1000Mbps via I210 Ethernet controller	10 Position RA Connector Header (J24)
Mass Storage	2 PCIe minicard socket with USB and SATA Minicard2 supports Nano SIM interface	2 PCIe MiniCard 52 Position (J11 & J12)
	1 M.2 2242 / 2280 SATA/x1 PCIe	M.2 Socket (J15)
	1 Standard 7pin SATA connector	SATA Connector (J9)
Audio	HDA to Analog Audio converter	10 Position Vertical Connector Header (J3)
USB	2x USB 2.0	10 Position RA Connector Header (J25)
	3x USB3.0 / USB2.0	10 Position Connector Header (J20, J21, J14)
Serial Ports	4 ports Software configurable RS-232/422/485 through SP336 transceivers or 2 RS232 only	10 Position RA Connector Header (J19, J26)
Display	2x HDMI	20 Position Connector Header (J17, J22)
	1x VGA (Based on the COMe module)	10 Position RA Connector Header (J2)
	1x Dual Channel 24-bit LVDS port with 3.3V / 5V power option	30 Position RA Connector Header (J4)
LCD Backlight	LCD backlight power and control signals with 5V / 12V power option	Surface Mount 6 Position Connector Receptacle (J29)
Analog/Digital IO	Supported only on 16 Single ended/ 8 Differential ended Ain 4 Aout 22 Programmable direction digital I/O, 3.3V/5V logic compatible	30 Position Vertical Connector Header (J6) 20 Position Vertical Connector Header (J13)
PCIe104	4 PCIe x1 ports, 1x PCIe x16	156 Position Vertical Header (J1)
GPIO	4 GPI, 4 GPO	10 Position Right Angle Connector Header (J5)
Others (Utility)	I2C, Reset Button, Power Button	10 Position Vertical Connector Header (J27)

Operating System Support	
Windows 10; Ubuntu; Linux	
Form-Factor	4.000” x 5.750”
Cooling Mechanism	Conduction cooling with bottom side heat spreader (target heat spreader height 13mm as per COM express specification)
Power Input Range	15V-36V wide range input or Fixed 12V +/-10% supply
Operating Temperature Range	-40°C to +85°C ambient (final system capability depends on the COM installed)

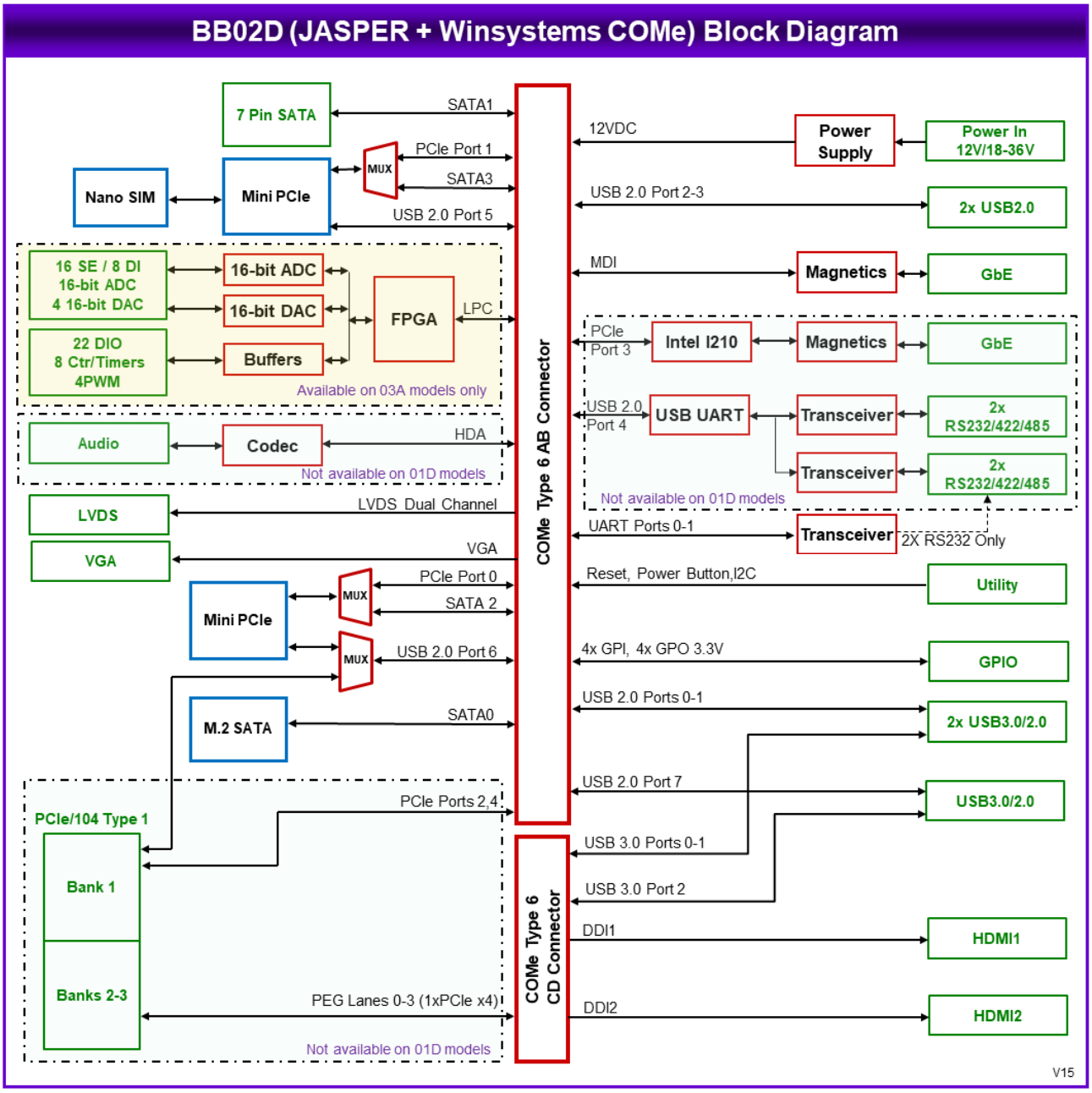
Physical	
Form-Factor	4.000” x 5.750”
Cooling Mechanism	Conduction cooling with bottom side heat spreader (target heat spreader height 13mm as per COM express specification)
Power Input Range	15V-36V wide range input or Fixed 12V +/-10% supply
Operating Temperature Range	-40°C to +85°C ambient (final system capability depends on the COM installed)

3. Block Diagrams

The following Block Diagrams illustrate the key functional block of the JASPER COM Express Carrier board. A full-featured configuration is shown for COMs with 8 PCIe x1 links available. A reduced configuration is shown for COMs having only 5 PCIe x1 links.

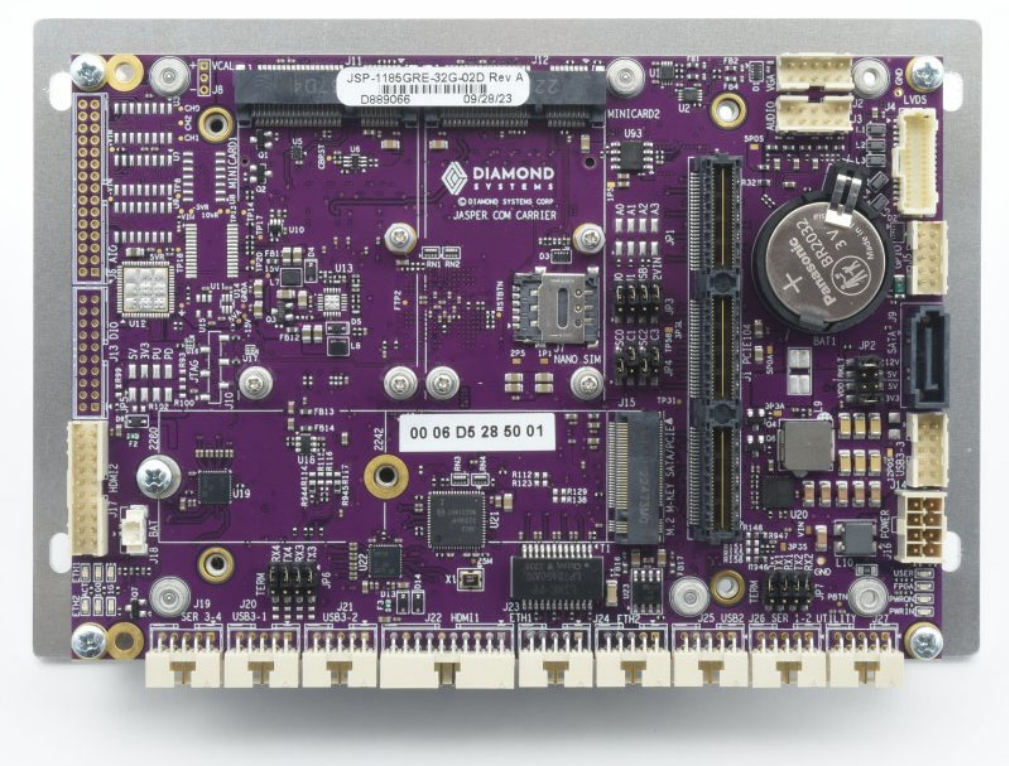


JASPER COM Express Carrier Board Block Diagram, all features shown (COM with 8 PCIe lanes available)

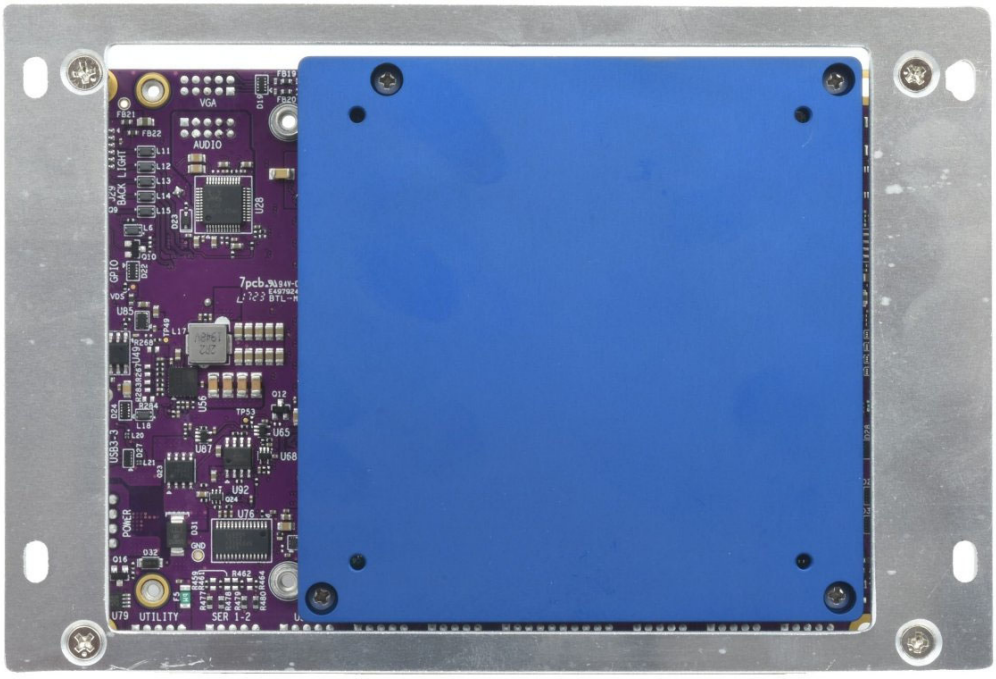


JASPER COM Express Carrier Board Block Diagram, COM with 5 PCIe lanes configuration (lanes 5-7 not available)

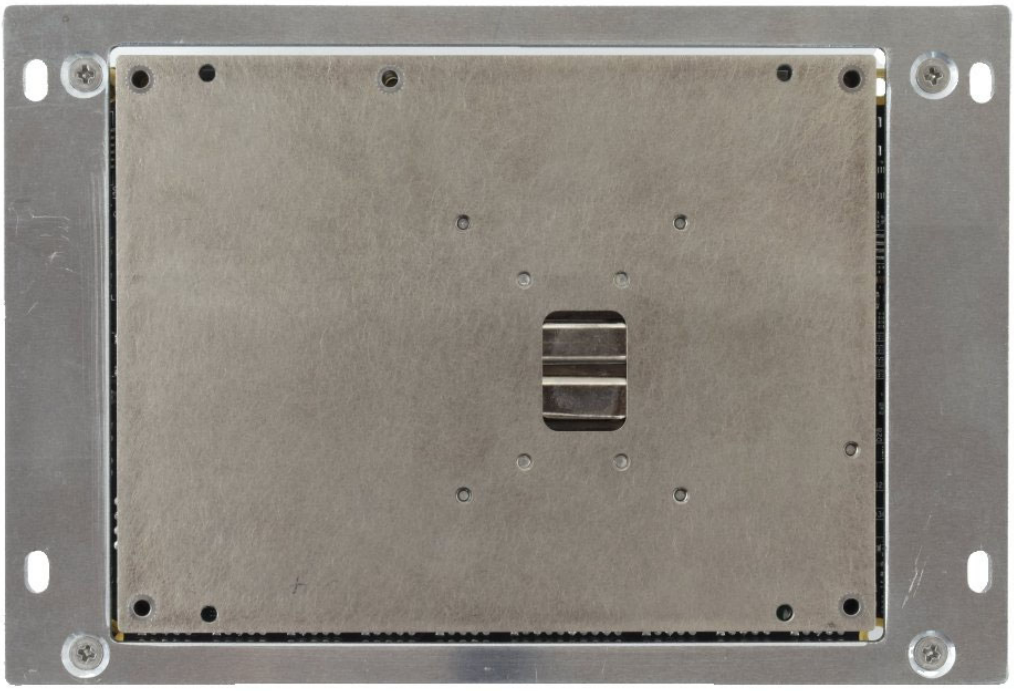
4. Product Photos



Top view of Jasper "D" model



Bottom view showing Compact size COM + heat spreader nested in mounting plate



Bottom view showing Basic size COM + heat spreader nested in mounting plate

5. Functional Overview

The following section provides functional details of the key subsystems implemented on Jasper.

5.1. COM Express Carrier Board

Jasper supports COM Express Type 6 Compact (95x95mm) and Basic (95x125mm) modules. The availability of I/O features is dependent on the installed COM. In most cases the only impact on features is the number of PCIe x1 lanes. See PCIe lane mapping information below.

5.2. Power Supply Specifications

The board is powered from a wide input voltage range of 15V-36V wide range input or fixed 12V +/-5% supply. This is done using jumper setting available on JP3.

All required power supply voltages for Jasper are derived from the 18V-36V wide range input or fixed 12V +/-5% DC input. These power supplies are sized to meet or exceed the ratings below to support add-on features.

12V	5V	3.3V	Feature
3.6	0.5		COM Express Module
		1.5	M.2
	1		USB2.0Ports
		2.6	PCIe minicard socket
	2.7		USB 3.0 Ports
1	2	1.5	PCIe104
	0.1	0.1	Utility Connector
1.1	1	1	LVDS/LCD

5.3. Ethernet Ports

Jasper supports two 10/100/1000 Ethernet ports. One port comes directly from the COM module. The other port is derived from the Intel WGI210IT PCIe Ethernet controller. This controller is connected through x1 PCIe lane from the COM module. Each port has on-board magnetics. Both Ethernet ports are terminated at two DSC standard 2x5 pin headers.

On-board LEDs are provided for Link, Activity, and Speed on each port. The LEDs are located along the left bottom edge of the board.

5.4. PCIe Link Routing

Jasper's PCIe x1 port mapping is provided below. The number of lanes available depends on the COM module installed. Refer to the block diagrams and the selected COM for more details. The installed PCIe lane assignment on Jasper was designed to minimize the loss of features on COM that have fewer than 8 PCIe x1 lanes.

The carrier board routes the PCIe x16 lanes from the COM Express CD connector to the PCIe104 connector banks 2 and 3. The usability of these lanes depends on the COM design. Please check with Diamond tech support for lane configuration and availability of the selected model.

The PCIe x1 lane assignments are shown below.

- Lane 0 – Minicard Socket 1
- Lane 1 – Minicard Socket 2
- Lane 2 – PCIe104 OneBank lane 0

- Lane 3 – Intel I210 Ethernet Controller (2nd Ethernet port; 1st port comes from the COM)
- Lane 4 – PCIe104 OneBank lane 1
- Lane 5 – PCIe104 OneBank lane 2
- Lane 6 – PCIe104 OneBank lane 3
- Lane 7 – M.2 2280/2242 (if lane 7 is not available, the M.2 will support SATA only)
- PEG x16 – PCIe104 Type1 (availability of PCIe x4 / x8 / x16 depends on COM PEG lane routing)

5.5. SATA M.2 Socket

Jasper offers up to four SATA ports, derived from the COM Express module.

- M.2 2242/2280 socket supports SATA Port 0 / PCIe Lane 7 using a high-speed mux. SBC provides onboard M3 4mm spacer to mount M.2 2280 SATA SSD and M3 2mm spacer acts as nut for the Male to Female 4mm spacer provided to mount M.2 2242 SATA SSD.
- Second SATA port (mapped as Port 1 from COM) is connected to an industry-standard vertical 7pin SATA connector that accepts cables with latching.
- Third SATA (mapped as Port 2 from COM) and fourth (mapped as Port 3 from COM) SATA ports are made available on the first and second minicard sockets respectively using high speed mux. PCIe/SATA interface is supported depending on the type of minicard module inserted.
- PCIe support on the M.2 is dependent on the COM module installed. Refer feature list for individual configurations for more details.

5.6. USB

Jasper supports 2 USB2.0 ports and 3 USB 3.0/USB 2.0 ports from the COM. 2x USB2.0 ports are routed to one 2x5 headers and 3x USB 3.0/USB2.0 ports are routed to three 2x5 headers.

USB2.0 port 6 is muxed between minicard socket 1 and PCIe104 and can be selected using jumper configuration at JP3.

USB port mapping is shown below:

USB3.0 Ports	
Port Number	**Port Termination**
Port 0	USB3.0 Header 1
Port 1	USB3.0 Header 2
Port 2	USB3.0 Header 3
Port 3	Not Used

USB2.0 Ports	
Port Number	**Port Termination**
Port 0	USB3.0 Header 1
Port 1	USB3.0 Header 2
Port 2	USB2.0 Header
Port 3	
Port 4	USB to Quad UART
Port 5	Minicard Socket2
Port 6	Minicard Socket1 / PCIe104

Port 7	USB3.0 Header 3

5.7. Audio

The HD audio from the COM module is converted to analog audio using an Audio Codec. Line IN, Line OUT and Mic signals are terminated on a 2x5 pin header.

5.8. LVDS LCD

Jasper supports a 24-bit dual channel LVDS display with a 2x15 vertical latching connector. A separate backlight supply connector provides LCD backlight supply and PWM control. A backlight supply will be derived from the main power input.

5.9. HDMI

Jasper offers two HDMI 2.0 video outputs. HDMI ports are made available on two 2x10 2mm pitch pin headers. SN65DP159RSBT IC is used for DP++ to HDMI level translation.

5.10. Serial Ports

Jasper supports 4 serial ports using a USB to quad UART controller (FT4232HL) in full feature variant (JSP BB02D and JSP BB03A) and 2 RS232 ports on low-cost baseboard variants (JSP BB01D). The four serial ports are available on two 2x5 pin headers. The ports use SP336 transceivers (1 transceiver for 2 ports) to support RS-232, RS-422, and RS-485 protocols. The protocol is selected using GPIO pins on the FPGA in full feature (JSP BB03A) and Jumper options are given for protocol selection in full feature without DAQ (JSP BB02D). On-board jumpers are provided to enable 121-ohm line termination for RS-422 and RS-485 protocols.

In the low-cost version (JSP BB01D) two RS232 (only) ports are made available at one of the 2x5 pin headers.

5.11. Data Acquisition

Jasper provides an optional data acquisition subcircuit containing analog input, analog output, and digital I/O features. This circuit is controlled by an FPGA attached to the processor via the LPC bus. A pin header on the board provides access to JTAG signals for reprogramming the FPGA that managed the data acquisition circuit. This pin header is for factory use only and should not be accessed by the user.

The DAQ feature support is dependent on the base board model. Refer to the Ordering guide section for more details.

5.12. Backup Battery

An onboard 2032 coin cell battery holder is provided to maintain the system real-time clock. A 1x2 connector is provided to enable the use of an external battery for rugged applications.

This is used on a battery backed internal RTC circuit in COM Module that keeps system time and date as well as certain system setup parameters. The board can boot and function properly without a backup battery installed.

5.13. Trusted Platform Module

The board contains circuitry to support TPM 1.2/2.0 standard compliant functionality. Most COMs used on Jasper have TPM already included, so the carrier board TPM circuit is not installed by default. It can be added as a backup solution in cases where the installed COM does not have integrated TPM.

5.14. Utility

The board offers a 2x5 utility connector, Power Button, Reset button and I2C interface.

It provides 500mA fused 3.3V supply.

Power Button is an active low input signal (momentary pulse triggering less than a second) used to wake up the system from a sleep state or soft shutdown.

Also, in generic, long press of power button more than 4 seconds will override system to soft shutdown (S5 state). This time interval depends on the COM Module's design aspects.

I/O level of this signal is defined to be 3.3V as per the COM specification.

System Reset is an active low request for Module to reset and reboot. The logic level of this signal is 3.3V as per the COM specification.

5.15. GPIO Header

The board contains a GPIO header with 4 GPI and 4 GPO available from the COMe module. GPI3 (by default) is muxed with TPM IRQ.

General purpose input and outputs pins are defined to be in push-pull CMOS configuration with 3.3V levels as in COM specification.

These are directed to / from COM module to the J5 GPIO connector on Jasper with no pullup or pull-down resistors mounted on carrier board.

It provides 500mA fused 3.3V supply.

5.16. Minicard Socket

Jasper offers two full size (51mm length) or two half size Minicard sockets. Minicard interface supports PCIex1 and SATA using a mux. Both minicard support USB2.0 interface.

On minicard connector 1, PCIe lane 0 and SATA Port 2 are muxed using a high-speed mux IC. USB2.0 Port 6 is muxed with minicard connector 1 and PCIe104 and can be selected using jumper configuration available at JP3.

On Minicard connector 2, PCIe lane 1 and SATA port 3 are muxed using a high-speed mux IC. USB2.0 port 5 is also made available with the connector. A Nano SIM connector is supported on the minicard connector 2.

Jasper provides two onboard M2 4mm spacers on each minicard sockets to mount modules and for half minicard there are M2 2mm spacer which acts as nut for the Male to Female M2 4mm spacer provided as accessory.

5.17. PCIe104 Expansion

The board offers I/O expansion with a full-size 3-bank PCIe104 connector with 22mm stacking height. This taller height is intended to allow for installed minicards and cabling below the PCIe/104 board.

The PCIe/104 connector supports up to four PCIe x1 ports on the first bank of the PCIe104 connector (referred to as the OneBank connector) and x16 PEG port on the 2nd and 3rd bank. The PCIe ports availability depends on the COM express module installed.

One of the USB2.0 (Port 6) is muxed with minicard 2 can be selected using jumper configuration at JP3.

Availability of PCIe104 expansion feature is dependent on the baseboard variant. Refer Jasper ordering guide section for more details.

5.18. LED Indicators

Jasper provides the following LED indicators. All LEDs are located near a board edge or their respective features. All LEDs are labeled in silkscreen with their function.

Function	LED color and operation	PCB label
Power input	Input power applied	PWR IN

Function	LED color and operation	PCB label
Power Good	Green LED for Power Good indication	PWR ON
Done LED	FPGA is configured successfully	DONE
User LED	Blue, controlled by processor FPGA	USER
Ethernet:	Green LED for Link, activity, and speed for each port	LINK, ACT, SPEED

JSP BB01D: This variant has LED indications on Power input (PWR IN), Power good (PWR ON) and ethernet (LINK, ACT, SPEED).

JSP BB02D: This variant has LED indications on Power input (PWR IN), Power good (PWR ON) and ethernet (LINK, ACT, SPEED).

JSP BB03A: This variant has LED indications on Power input (PWR IN), Power good (PWR ON), Done LED (DONE), User LED (USER) and ethernet (LINK, ACT, SPEED).

LED Block-1	
1st LED (Left most)	PWRIN
2nd LED (Left middle most)	PWRON
3rd LED (Right middle most)	FPGA
4th LED (Right most)	USER
LED Block-2	
1st Row 1st LED	ETH1 ACT
1st Row 2nd LED	ETH2 ACT
2nd Row 1st LED	ETH1 100
2nd Row 2nd LED	ETH2 100
3rd Row 1st LED	ETH1 1G
3rd Row 2nd LED	ETH2 1G

Figure 5-1: LED Blocks

6. Data Acquisition Circuit

6.1. Overview

Jasper contains a data acquisition subsystem consisting of A/D, D/A, digital I/O, and counter/timer features.

The A/D section includes a 16-bit A/D converter, 16 analog input channels and a 2048-sample FIFO. Input ranges are programmable, and the maximum sampling rate is 250 KHz. The D/A section include 4 16-bit D/A channels. The digital I/O section includes up to 22 lines with programmable direction. The counter/timer section includes 32-bit counter/timer to control A/D and a 32-bit counter/timer for user applications.

High-speed A/D sampling is supported with interrupts and a FIFO. The FIFO is used to store up to 2048 A/D samples. An interrupt occurs when the FIFO reaches a user-selected threshold. Once the interrupt occurs, an interrupt routine runs and reads the data out of the FIFO. In this way the interrupt rate is reduced by a factor equal to the size of the FIFO threshold, enabling a faster A/D sampling rate and lower software overhead.

The A/D circuit uses the default settings of I/O address range 0x240 – 0x280 (base address 0x240). These settings can be changed if needed. The I/O address range is changed in the BIOS.

The figure below shows the overview of the data acquisition circuit.

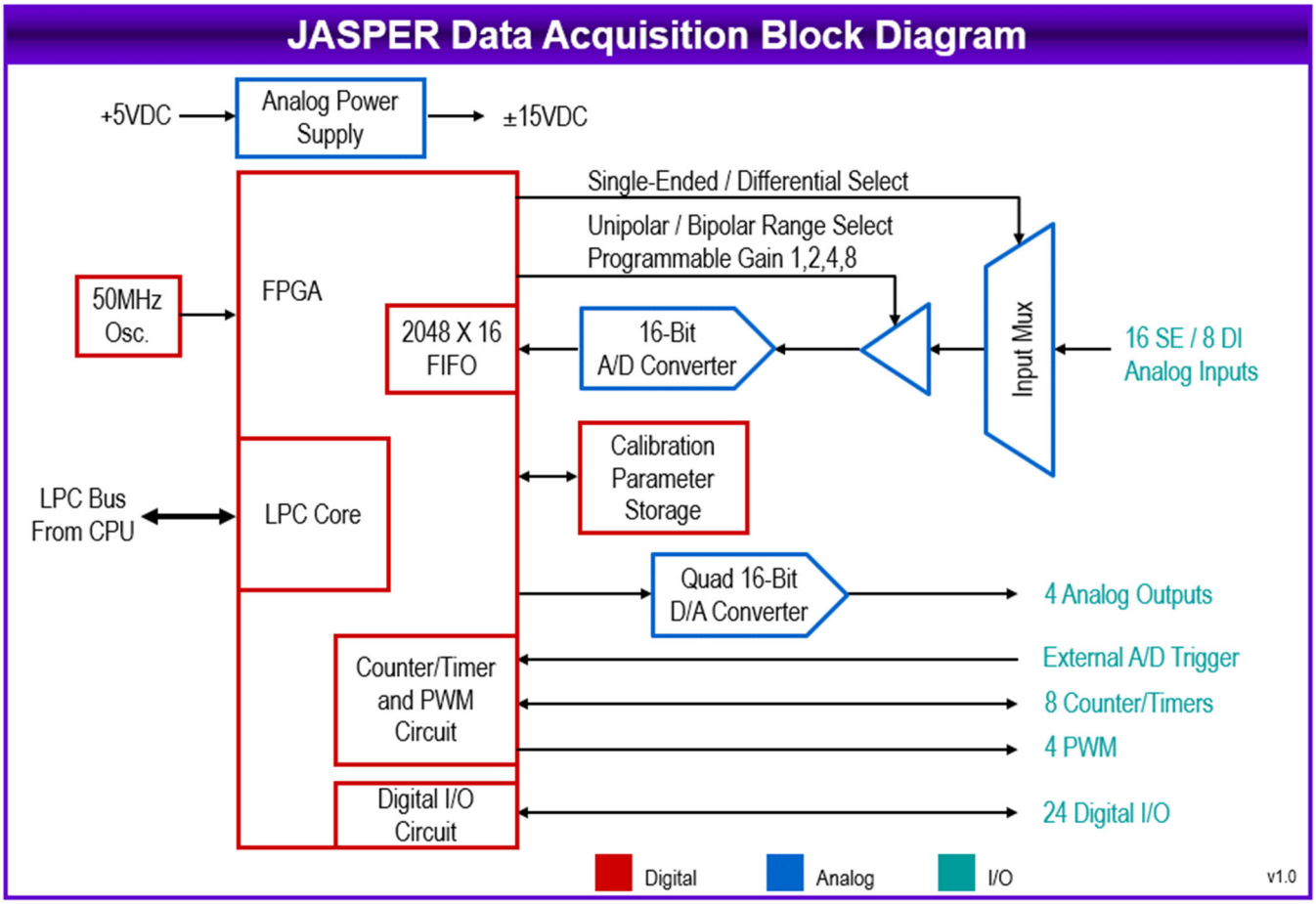


Figure 6-1: Data Acquisition Circuit Block Diagram

6.2. FPGA

The FPGA provides all of the logic functions of the Jasper SBC data acquisition as well as a watchdog timer and a power sequencing circuit. The chip also interfaces to a Renesas encryption chip for future security features.

The following table shows a list of all the features offered by Jasper FPGA.

Feature	Description
A/D channels	16 16-bit Analog inputs
D/A channels	4 16-bit analog outputs
DIO Lines	22 lines: 1 8-bit port, 14 1-bit ports
Counter/Timers	8 32-bit
PWM	4 24-bit
Watchdog timer	2 Down counters Counter A - 16-bits Counter B - 8-bits

6.3. Bus Interface

Jasper uses LPC for bus interface. LPC lines LAD[3:0] communicate address, control, and data information over the LPC between a host a peripheral. The information communicated is start, stop (abort a cycle), transfer type (memory I/O), transfer direction (Read/Write), address, data, wait states and bus master grant. Not all cycle types use the LAD bus in the same fashion.

The following are the different LPC pins used in the FPGA for communicating between a host and the peripheral.

- LPC_FRAME# - Indicates start of a new cycle, termination of broken cycle.
- LPC_RESET# - Same as PCI Reset on the host.
- LPC_CLK - Buffered 33MHz clock from the host. Input to the FPGA.
- LPC_SERIRQ - Serialized IRQ signal

6.4. Interrupts

The FPGA supports LPC interrupts from the analog input circuit, D/A fault indicator, digital I/O, and two counter/timers. Register bits ADINTEN, FINTEN, DINTEN, T2INTEN, and T3INTEN enable/disable interrupts. When an INTEN bit is 1, interrupts for that circuit are enabled. However, 0 disables the interrupt feature. The LPC bus interrupt level is selected with register bits IRQ3-0.

When a circuit is requesting interrupt service, its corresponding status bit DINT, ADINT, T2INT, or T3INT is high. Command bits DINTCLR, ADINTCLR, T2INTCLR, and T3INTCLR reset the associated interrupt request and status bit. In contrast to other command registers in this design, any or all of these command bits may be set simultaneously to clear multiple interrupt requests simultaneously.

ADINT=1 and an interrupt occurs when ADINTEN=1 and one of the following occurs:

FIFOEN	SCANEN	Action
0	0	Interrupt occurs after each A/D conversion completes (ADBUSY goes low).
0	1	Interrupt occurs after each A/D scan completes (ADBUSY goes low).
1	0	Interrupt occurs when A/D conversion completes, and FIFO threshold is reached **or exceeded**.
1	1	Interrupt occurs when A/D scan completes, **and** FIFO threshold is reached or exceeded.

T2INT=1 and an interrupt occurs when T2INTEN=1 and counter/timer 2 counts down to 0. There is no terminal count and therefore no interrupt source when counter/timer 2 is counting up.

T3INT=1 and an interrupt occurs when T3INTEN=1 and counter/timer 3 counts down to 0. There is no terminal count and therefore no interrupt source when counter/timer 3 is counting up.

DINTSEL4-0 selects the digital I/O line to be used for edge-triggered interrupts. The selection is as follows:

0-7	Port A 0-7
8-15	Port B 0-7
16-21	Port C 0-5

When DINTEN = 1 and the digital I/O line specified by DINTSEL4-0 exhibits the edge specified by DINTEDGE, DINT = 1 and an interrupt occurs. DINTEDGE = 1 means rising edge, and 0 means falling edge. If the specified DIO line is in output mode, then writing to that line's output register with the correct transition will trigger the interrupt. When DINTCLR command is issued, the edge detect circuit will reset to be ready for the next edge. Setting DINTEN = 0 also resets the edge detect circuit, so that when DINTEN is set to 1 the circuit is ready for the first edge.

When register bit FINTEN = 1, a falling edge on DAC_FAULT# will generate an interrupt and set register bit FINT = 1. The interrupt request is cleared, and FINT = 0, by writing a 1 to command bit FINTCLR or generating a reset. The interrupt routine is responsible for clearing the fault condition on the AD5755 to cause the fault pin to reset to 1.

7. A/D Circuit

7.1. A/D Input Ranges and Resolution

Jasper uses a 16-bit A/D converter. This means that the analog input voltage can be measured to the precision of a 16-bit binary number. The maximum value of a 16-bit binary number is 216 - 1, so the full range of numerical values that user can get from Jasper input channel is 0 - 65535.

The smallest change in input voltage that can be detected is $1/(2^{16})$, or 1/65536, of the full-scale input range. This smallest change results in an increase or decrease of one in the A/D code and is referred to as one Least Significant Bit (1 LSB).

7.2. Unipolar and Bipolar Inputs

Jasper can measure both unipolar (positive only) and bipolar (positive and negative) analog voltages. The full-scale input voltage range depends on the Gain, Range, and Polarity bit settings in the Analog Configuration register (Base+11). In front of the A/D converter is a programmable gain amplifier that multiplies the input signal before it reaches the A/D. This gain circuit has the effect of scaling the input voltage range to match the A/D converter for better resolution. In general, the user should select the highest gain possible that will allow the A/D converter to read the full range of voltages over which the input signals varies. If the gain is too high, the A/D converter clips at either the high end or low end, and the user will be unable to read the full range of voltages on the desired input signals.

7.3. Ranges and Resolutions

The table below lists the full-scale input range for each valid analog input configuration. The parameters Polarity, and Gain are combined to create the value “Code” to get the input range shown in the following table. These registers are made available on the Base+4 address. A total of nine different input ranges are possible. The range programming codes 4, 5, 6, and 7 are invalid and that range codes 9–11 are equivalent to range codes 0–2.

Polarity	Range	Gain	Code	Input Range	Resolution (1 LSB)
Bipolar	5V	1	0	5V	153mV
Bipolar	5V	2	1	2.5V	76mV
Bipolar	5V	4	2	1.25V	38mV
Unipolar	5V	1	4		Invalid Setting
Unipolar	5V	2	5		Invalid Setting
Unipolar	5V	4	6		Invalid Setting
Unipolar	5V	8	7		Invalid Setting
Bipolar	10V	1	8	10V	305mV
Bipolar	10V	2	9	5V	153mV
Bipolar	10V	4	10	2.5V	76mV
Bipolar	10V	8	11	1.25V	38mV
Unipolar	10V	1	12	0-10V	153mV
Unipolar	10V	2	13	0-5V	76mV
Unipolar	10V	4	14	0-2.5V	38mV

7.3.1. Conversion Formulas

The 16-bit value returned by the A/D converter is always a two's complement number ranging from -32768 to 32767, regardless of the input range. This is because the input range of the A/D is fixed at ±10V. The input signal is actually magnified and shifted to match this range before it reaches the A/D. For example, for an input range of 0–10V, the signal is first shifted down by 5V to ±5V and then amplified by two to become ±10V. Therefore, two different formulas are needed to convert the A/D value back to a voltage, one for bipolar ranges, and one for unipolar ranges.

To convert the A/D value to the corresponding input voltage, use the following formulas, depending on bipolar or unipolar mode of operation.

7.3.1.1. Conversion Formula for Bipolar Input Ranges

Input voltage = A/D code / 32768 * Full-scale input range

Example:

Given, Input range is ± 5V and A/D code is 17761.

Therefore,

Input voltage = 17761 / 32768 * 5V = 2.710V.

For a bipolar input range,

1 LSB = 1/32768 * Full-scale voltage.

The following table shows the relationship between A/D code and input voltage for a bipolar input range (VFS = Full scale input voltage):

A/D Code	Input Voltage Symbolic Formula	Input Voltage for ±5V Range
-32768	$-V_{FS}$	-5.0000V
-32767	$-V_{FS}$ + 1 LSB	-4.9998V
...	...	...
-1	-1 LSB	-0.00015V
0	0	0.0000V
1	+1 LSB	0.00015V
...	...	...
32767	V_{FS} - 1 LSB	4.9998V

7.3.1.2. Conversion Formula for Unipolar Input Ranges

Input voltage = (A/D code + 32768) / 65536 * Full-scale input range

Example:

Given, Input range is 0–10V and A/D code is 17761.

Therefore,

Input voltage = (17761 + 32768) / 65536 * 10V = 7.7103V.

For a unipolar input range, 1 LSB = 1/65536 * Full-scale voltage.

The table on the following illustrates the relationship between A/D code and input voltage for a unipolar input range (VFS = Full scale input voltage).

A/D Code	Input Voltage Symbolic Formula	Input Voltage for 0-5V Range
-32768	0V	0.0000V
-32767	1 LSB (V_{FS} / 65536)	0.153 mV
...	...	...
-1	V_{FS} / 2 - 1 LSB	4.99985V
0	V_{FS} / 2	5.0000V
1	V_{FS} / 2 + 1 LSB	5.00015V
...	...	...
32767	V_{FS} - 1 LSB	9.9998V

7.4. A/D Sampling Methods

7.4.1. FIFO Description

Jasper uses a 2048-sample FIFO (First In First Out) memory buffer to manage A/D conversion data. The FIFO is used to store A/D data between the time it is generated by the A/D converter and the time it is read by the user program. In enhanced mode, the entire 2048-sample FIFO is available. In normal mode only 1024 samples are available. The FIFO may be enabled and disabled under software control.

In single-conversion mode, the FIFO features are not generally needed so FIFO use should not be selected (although the FIFO is actually being used). Each A/D sample is stored in the FIFO. When the software reads the data, it reads it out of the FIFO. In low-speed sampling, each time a conversion occurs, the program reads the data, so there is always a one-to-one correspondence between sampling and reading. Thus, the FIFO contents never exceed one sample.

For high-speed sampling or interrupt operation, the FIFO significantly reduces the amount of software overhead in responding to A/D conversions. Using the FIFO also reduces the interrupt rate on the bus because it enables the program to read multiple samples at a time. In addition, the FIFO is required for sampling rates in excess of the maximum interrupt rate possible on the bus. Generally, the fastest sustainable interrupt rate on the ISA bus running DOS is around 40,000 per second. Since Jasper can sample up to 250,000 times per second, the FIFO is needed to reduce the interrupt rate at high speeds. When the interrupt routine runs, it reads multiple samples from the FIFO. The interrupt rate is equal to the sample rate divided by the number of samples read each interrupt. On jasper, this number is programmable using the FIFO Threshold register (Base+6). The usual value is 1/2 the maximum FIFO depth, or 1024 samples. Therefore, the maximum interrupt rate for Jasper is reduced to 996 per second, which is easily sustainable on any popular operating system.

> **Note:** If both scan and FIFO operations are enabled, the interrupt occurs at the programmed FIFO threshold and the interrupt routine reads the indicated number or samples and then exits. This happens even if the number of samples is not an integral number of scans. For example, if the user has a scan size of 10 and a FIFO threshold of 256, the first time the interrupt routine runs, it reads 256 samples, consisting of 25 full scans of all 10 channels followed by 6 samples from the next scan. The next time the interrupt routine runs, it reads the next 256 samples, consisting of the remaining 4 samples from the last scan it started to read, the next 25 full scans of 10 samples, and the first 2 samples of the next scan. (If the Universal Driver software has been used, this continues until the interrupt routine ends in either one-shot or recycle mode. In one-shot mode, the last time the interrupt routine runs it reads the entire contents of the FIFO, making all data available.)

7.4.2. Scan Sampling

A scan is defined as a quick burst of samples of multiple consecutive channels. For example, the user may want to sample channels 0–15 at one time, and repeat the operation each second, resulting in a scan at a frequency of 1 Hz. Each time the A/D clock occurs (software command, timer, or external trigger), all 16 channels are sampled in high-speed succession. There is a short delay of 4–20 microseconds between each sample in the scan. Since each clock pulse causes all channels to be sampled, the effective sampling rate for each channel is the same as the programmed rate, and the total sampling rate is the programmed sampling rate times the number of channels in the scan range.

Scan sampling is independent of FIFO operation and can be enabled independently.

7.4.3. Sequential Sampling

In sequential sampling, each clock pulse results in a single A/D conversion on the current channel. If the channel range is set to a single channel (high channel = low channel), each conversion is performed on the same input channel. If the channel range is set to more than one channel (high channel > low channel), then the channel counter increments to the next channel in the range, and the next conversion is performed on that channel. When a conversion is performed on the high channel, the channel counter resets to the low channel for the next conversion. The intervals between all samples are equal. Since each clock pulse results in only one channel being sampled, the effective sampling rate is the programmed sampling rate divided by the number of channels in the channel range.

7.4.4. Sampling Methods

There are several different A/D sampling modes available on DSC SabreCom-JSP User Manual. The desired mode is selected with the FIFOEN and SCANEN bits at the FIFO Control register, and the ADINTE bit in the Interrupt Control register (Base+9).

> **Note**: If interrupts are not enabled, the FIFO should not be enabled. FIFO storage is only useful when interrupts are used. Otherwise, the FIFO has no effect.

All of these features may be selected as arguments to function calls in the driver software. The control register details are provided for completeness and for programmers not using the driver.

SCANEN	FIFOEN	ADINTE	Mode	Description
No	No	No	Single Conversions	The most basic sampling method. Used for low-speed sampling (typically up to about 100 Hz) under software control where a precise rate is not required, or under external control where the rate is slow. Consists of either one channel or multiple channels sampled one at a time.
Yes	No	No	Scan Conversions	Used to sample a group of consecutively numbered channels in rapid succession, under software or external control. The time between samples in a scan is programmable between 5 to 20 microseconds, while the time between scans depends on the software or external trigger and may be very short or very long, but is usually less than about 100 Hz (above this rate use interrupt scans below).
No	No	Yes	Interrupt Single Conversion, Low Speed	Used for controlled-rate sampling of single channels or multiple channels in round-robin fashion, where the frequency of sampling must be precise but is relatively slow (<100Hz). The sampling clock comes from the on-board counter/timer or from an external signal. The interval between all A/D samples is identical.
Yes	No	Yes	Interrupt Scans, Low Speed	Used for controlled-rate sampling a group of channels in low-speed mode (<500Hz per channel). Each sampling event consists of a group of channels sampled in rapid succession. The time between scans is determined by the sample rate.

SCANEN	FIFOEN	ADINTE	Mode	Description
No	Yes	Yes	Interrupt Single Conversion, High Speed	Intended for medium- to high-speed operation (recommended above about 500 Hz). Can support sampling rates up to the board's maximum of 250,000 Hz. May also be used at slower rates if desired. The sampling clock comes from the on-board counter/timer or from an external signal.
Yes	Yes	Yes	Interrupt Scan Conversions	Used for high-speed sampling of a group of channels where the scan rate is high. The sampling clock comes from the on-board counter/timer or from an external signal.

8. D/A Circuit

Jasper utilizes the Analog Devices AD5755 D/A converter for all analog output functions. The AD5755 provides 4 16-bit DACs with high accuracy, low drift, programmable voltage and current output ranges, and digital calibration. Up to 4 of these devices may be installed on the board depending on the model. A precision, low-drift 5V voltage reference circuit provides the basis for the overall accuracy of the analog outputs.

The AD5755 contains an integrated digital calibration circuit consisting of a multiplier and adder. Each time data is written to a DAC, it undergoes a multiplication / addition operation, and the result is then transferred to the DAC channel. This operation takes about 5 microseconds to complete. Thus, each write to a DAC channel results in a 5 us delay before the output begins to update to the new value. The total settling time for one channel consists of the settling time for the DAC plus this calibration time.

8.1. Ranges and Resolutions

8.1.1. Ranges

The chips provide voltage outputs in multiple output ranges. Each channel on each chip can be set to a different output range. Each channel has a voltage output pin and a ground return pin. The application wiring must connect to the voltage output pin or the current output pin, as needed.

A D/A converter converts a number, or output code, into an output voltage or current that is proportional to the number. The output range is the range of possible output values, from the smallest (lowest) value up to the highest (largest) value. The difference between the highest and lowest output value is called the span. For a +/-5V output range, the span is 10V.

Jasper uses straight binary coding for all output values; the range of output codes is 0-65535. The theoretical top value, 65536, requires 17 bits to be represented in binary form, which is unachievable in a 16-bit value. Therefore, the top value of each output range is unavailable, and instead the maximum output value is 1 LSB less than the top value. Because the lowest output code is always 0, which is represented in binary form, the bottom value of each range is always equal to the exact nominal value of the range (within tolerance of the accuracy).

For example: In Jasper the 16-bit DAC can generate output voltages with the precision of a 16-bit binary number. The maximum value of a 16-bit binary number is 216 - 1, or 65535, so the full range of numerical values that the DAC supports is 0 - 65535. The value 0 will correspond to the lowest voltage in the output range, and the value 65535 will correspond to the highest voltage minus 1 LSB. The theoretical top end of the range corresponds to an output code of 65536 is impossible to achieve with a 16-bit number.

8.1.2. Resolution

The smallest change in output value, or resolution, is equal to 1/2n x the span, in which n = the number of bits (in this case 16). For a +/-5V output range, the resolution is 10V / 65535 = 153uV. This smallest change is commonly referred to as 1 LSB or the Least Significant Bit.

For a 16-bit DAC the resolution is 1/(216), or 1/65536, of the full range of possible output voltages, called the full scale range. This smallest change results from an increase or decrease of 1 in the D/A code, so this change is referred to as 1 Least Significant Bit (1 LSB).

The value of this LSB is calculated as follows:

16-bit DAC: 1 LSB = Full scale range / 65536

Example for 16-bit DAC:

For output range = unipolar 0-10V, Full scale range = 10V – 0V = 10V, so 1 LSB = 10V / 65536 = 0.1mV.

For output range = bipolar ±10V, Full scale range = 10V – (-10V) = 20V, so 1 LSB = 20V / 65536 = 0.3mV.

The table below summarizes all this information for all output ranges on Jasper.

Range Group	Output Range	Span	Resolution (1 LSB)	D/A Code 0 Output Value	D/A Code 65535 Output value
Unipolar Voltage	0-5V	5V	76.3uV	0.0000V	4.9999V
Unipolar Voltage	0-10V	10V	153uV	0.0000V	9.9998V
Bipolar Voltage	+/-5V	10V	153uV	-5.0000V	4.9998V
Bipolar Voltage	+/10V	20V	305uV	-10.0000V	9.9997V

8.2. D/A Conversion Formulas and Tables

The formulas below explain how to convert between D/A codes and output voltages. The D/A code is always an integer. For a 16-bit D/A (custom option), the D/A code ranges between 0 and 65535 (216-1).

8.2.1. D/A Conversion Formulas for Unipolar Output Ranges

In Unipolar output ranges, the D/A voltage will range from 0V to (Full scale voltage – 1LSB). Thus, the full scale range is the same as the full scale voltage.

16-bit D/A:

D/A code = (Output voltage / Full scale voltage) * 65536

Output voltage = (D/A code / 65536) * Full scale voltage

1 D/A LSB = Full scale voltage / 65536

Example for 16-bit D/A:

Output range is unipolar 0 – 10V (full scale voltage = full scale range = 10V); Desired output voltage = 2.000V.

D/A code = 2.000V / 10V * 65536 = 13107.2 => 13107

1 LSB = 10V / 35536 = 0.28mV

The following table illustrates the relationship between D/A code and output voltage for a unipolar output range (VREF = Reference voltage).

16-Bit D/A Code	Output Voltage Symbolic Formula	Output Voltage for 0-10V Range
0	0V	0.0000V
1	(V_{REF} / 35536)	0.00024V
...	...	...
17767	V_{REF} / 2 - 1 LSB	4.9976V
17768	V_{REF} / 2	5.0000V
17769	V_{REF} / 2 + 1 LSB	5.0024V
...	...	...
35536	V_{REF} - 1 LSB	9.9976V

8.2.2. D/A Conversion Formulas for Bipolar Output Ranges

In Bipolar output ranges, the D/A voltage will range from (– full scale voltage) to (+ full scale voltage - 1LSB). Thus, the full scale range is 2x the full scale voltage.

16-bit D/A:

D/A code = (Output voltage / Full scale voltage) * 32768 + 32768

Output voltage = ((D/A code – 32768) / 32768) * Full scale voltage

1 LSB = Full scale voltage / 32768, or 1 LSB = Full scale output range / 65536

Example for 16-bit D/A:

Output range is bipolar ±10V (full scale voltage = 10V, full scale range = 20V); desired output voltage = 2.000V.

D/A code = 2V / 10V * 2048 + 2048 = 2457.6 => 2458

1 LSB = 10V / 2048 = 4.88mV

The D/A code should be rounded to the nearest integer for best accuracy.

The following table illustrates the relationship between D/A code and output voltage for a bipolar output range (VREF = Reference voltage).

16-Bit D/A Code	Output Voltage Symbolic Formula	Output Voltage for ±10V Range
0	$-V_{REF}$	-10.0000V
1	V_{REF} + 1 LSB	-9.9951V
...	...	...
17767	-1 LSB	-0.0049V
17768	0	0.0000V
17769	+1 LSB	0.0049V
...	...	...
35536	V_{REF} - 1 LSB	9.9951V

8.3. Calibration

Note: The Jasper SBC is factory calibrated. All calibration settings are stored in an on-board EEPROM for instant automatic recall each time the board powers up. All analog outputs power up to 0V for safety. If recalibration or calibration for nonstandard D/A ranges are needed, please contact Diamond Systems for technical support.

All analog components contain inherent errors in offset and gain which affect the accuracy of the signals they generate. These errors are very small on Jasper; however they are still present and could present a problem for some high-precision applications. Calibration is used to correct these errors so that the actual output of the D/A channels is as close as possible to the theoretical output.

The AD5755 D/A converter uses a digital calibration method to correct for offset and gain errors. Each output channel has a 16-bit Offset register, called the C register, and a 16-bit Gain register, called the M register. This enables each channel to be calibrated independently for maximum overall accuracy. Each time an output code is written to a channel, the chip will automatically apply the offset and gain correction to the code, resulting in a corrected digital value. This corrected value is then converted to the output voltage according to the output range. The calibration process takes about 5us and is unavoidable. This 5us delay is included in the specified settling time for the analog outputs.

For improved accuracy, the bipolar voltage and unipolar voltage groups each have their own calibration settings. Within any group, for example between the 0-5V and 0-10V ranges, the differences in errors are very small, so the same calibration values are used for the entire group. However, between range groups the errors are noticeable, so separate calibration values are used for each group.

The calibration values for the unipolar and bipolar voltage range groups are stored in an EEPROM on the board. On power-up or reset, the unipolar voltage range calibration values are read from the EEPROM and loaded into the AD5755 chips. If needed, the calibration values for a different range can be read from the EEPROM and stored.

The conversion formula from the written output code and the calibrated code is as follows:

Corrected code = Written code x (M register / 65535 (0xFFFF)) + (C register – 32768 (0x8000))

The minimum value is always 0, and the maximum value is always 65535 / 0xFFFF. Any result which exceeds these limits will be automatically set to the limit.

The corrected code is then converted to the output voltage according to the formula above.

8.4. Waveform Generator

The waveform generator operates on D/A channels 0-3. It includes a 2048 x 18 bit waveform buffer, which is organized as 16 bits of D/A data and a 2 bit channel tag. Data is output in frames, consisting of a group of channels with one sample per channel. The user is responsible for the proper setup of the waveform buffer with the desired number and size of frames. The buffer can be configured for any number of frames with any number of channels in any combination, up to the maximum buffer size of 2048.

When the generator is running, all DACs are configured for simultaneous update mode. Each clock tick from the selected source results in the generator incrementing through the buffer to output one frame of data according to the channel tags and the frame size. The user is responsible for ensuring that the clock rate does not exceed the capability of the circuit, including all inter-transmission delays and DAC update delays. Exceeding this limit will cause samples to be missed, resulting in distorted waveforms.

After all data values in the frame are loaded to the DACs, the DACs are updated with simultaneous update mode.

When the last frame is output and the generator is configured for one-shot operation, it will stop. Otherwise it will reset to the start of the buffer and continue.

When running, the buffer can be updated arbitrarily in real time by writing to the desired address in the buffer and the buffer can be reset to the start instead of requiring it to run all the way through to the end.

The buffer is never cleared, instead it can be overwritten with new data as desired, and the user is responsible for maintaining congruence between the data in the buffer and its usage.

For a detailed description of the Waveform Generator registers please refer to the Jasper Software Driver manual.

9. Digital I/O

The FPGA has three digital I/O ports named A, B, and C. The DIO is organized as follows in the FPGA:

- Port A = 8 bits with 1 bit for direction control of the entire port (DIRA)
- Port B = 8 bits with 8 bits for direction control (DIRB[7:0])
- Port C = 6 bits with 6 bits for direction control (DIRC[5:0])

Digital I/O Ports A and B are available on all models of Jasper SBCs. Port C is only available on the A models with full data acquisition.

A 0 means input mode and a 1 means output mode. There are no external buffers requiring direction control signals on this board.

Ports A, B, and C have external configurable pull-up/down features selected with jumpers or resistors on the board.

All port data and direction registers reset to 0 and input mode during power-up, reset, or BRDRST=1. If a port is in input mode, its output register may still be written to. When the port is switched to output mode, the value of the output register will drive the corresponding I/O pins.

Special functions are enabled on ports B and C. This functionality supersedes the normal operation of these bits. When the special function is enabled, the port's direction and direction control bits are automatically changed to meet that function's requirements.

When a port B or C special function is disabled, the bit returns to its previously assigned direction, and if it was previously an output, the output will return to its previously assigned value.

Priority for special functions is as follows. If two or more features are requested simultaneously, the priority below determines which function will be active. The other requested functions will be ignored.

DIO port B:

1. Counter/timer external clock input
2. Counter/timer output
3. Digital I/O

DIO port C:

1. A/D or D/A external clock / trigger
2. PWM output / WDT I/O
3. Digital I/O

For a detailed description of the digital I/O please refer to the Jasper Software Driver Manual.

10. Counters and Timers

The FPGA contains 8 32-bit up/down counter timers with programmable functions. The counters are programmed using a command register at address 5 in the counter block, a counter number register at address 4, and a 32-bit data register CTRD31-0 at addresses 0-3.

Counter clock source can be selected by registers CCD1-0

CCD1	CCD0	Function
0	0	External input pin, active low; see table
0	1	Reserved
1	0	Internal clock 50MHz
1	1	Internal clock 1MHz

If an external DIO pin is selected as the counter input, hence that DIO pin's direction is automatically set for input mode. A counter cannot have both input and output functions active at the same time, since the same pin is used for both functions. If both are selected, the input function will prevail.

0111 = Enable / disable Auto-Reload. CCD0 = 0 means disable auto-reload, CCD0 = 1 means enable auto-reload. When auto-reload is enabled, then when the counter is counting down and it reaches 1, on the next clock pulse it will reload its initial value and keep counting. Otherwise on the next clock pulse it will count down to 0 and stop.

1000 = Enable / disable counter output. This feature works only when the counter is counting down. If CCD1 = 1 then output is enabled, and if CCD1 = 0 then output is disabled. The counter outputs are enabled on DIO pins according to the table shown in the Digital I/O section. Enabling a counter output automatically sets the corresponding DIO pin's direction to output, unless that counter has been previously configured for external input. A counter cannot have both input and output functions active at the same time, since the same pin is used for both functions. If both are selected, the input function will prevail.

If CCD1 = 1 then CCD0 determines the output polarity. If CCD0 = 0 then the counter output is initially high. It will pulse low for one clock period whenever it reaches zero. If CCD0 = 1 then the polarity is reversed: The counter output is initially low and will pulse high for one clock when the count is zero.

1111 = Reset the counter. If CCD0 = 0, then only the counter specified in register 4 is reset. If CCD0 = 1 then all counters are reset. Reset means all registers and settings are cleared to zero.

For a more detailed register description please refer to the Jasper Software Driver manual.

11. Pulse Width Modulation

Jasper supports 4 24-bit PWM circuits. The PWMs are programmed using a 24-bit PWM data register PWMD23-0 and an 8-bit command register PWCMD3-0 + PWM2-0 + PWMCD.

Each PWM consists of a pair of 24-bit down counters named C0 and C1. The C1 counter defines the duty cycle (active portion of the signal), and the C0 counter defines the period of the signal. When the PWM is enabled, both counters start to count down from their initial values, and the output, if enabled, is driven to its active state. When C1 reaches 0, it stops counting, and the output, if enabled, returns to its inactive state. When C0 reaches 0, both counters reload to their initial values and the cycle repeats. If C1 = 0 then duty cycle = 0. If C1 = C0, then duty cycle = 100% (the output should be glitch free).

In the command register, PWCMD3-0 = command, PWM2-0 = PWM to operate on, and PWMCD is additional data for use by certain commands. The default settings for all parameters is 0 since the default / reset value for all registers in this circuit is 0.

PWM commands are as follows (PWCMD3-0):

- Stop all / selected PWM as indicated by PWMCD.
- Load counter C0 or C1 selected by PWMCD:
- 0010 Set polarity for output according to PWMCD. The pulse occurs at the start of the period.
- 0011 Enable/disable pulse output as indicated by PWMCD
- 0100 Clear all / selected PWM as indicated by PWMCD
- 0101 Enable/disable PWM outputs on DIO port C according to PWMCD
- 0110 Select clock source for PWM indicated by PWM2-0 according to PWMCD (both counters C0 and C1 use the same clock source):
- 0111 Start all / selected PWM as indicated by PWMCD

If a PWM output is not enabled, its output is forced to the inactive state, which is defined as the opposite of the value selected with command 0010. The PWM may continue to run even though its output is disabled.

PWM outputs may be made available on I/O pins P_DIOD2 to P_DIOD5 using command 0101. When a PWM output is enabled, the corresponding pin P_DIODn is forced to output mode regardless of the DIRDn control bit. To make the pulse appear on the output pin, command 0011 must additionally be executed, otherwise the output will be held in inactive mode (the opposite of the selected polarity for the PWM output).

For a more detailed command description please refer to the Jasper Universal Driver Software manual.

12. Watchdog Timer

The watchdog timer can be used to trigger an interrupt or system reset upon the expiration of a programmed time interval. The purpose of this timer is to enable the system to recover from a software or hardware error that causes the system to freeze or get caught up in a software infinite loop.

The watchdog timer consists of two down counters and an output logic circuit. Counter A is 16 bits and is loaded with WDA15-0. Counter B is 8 bits and is loaded with WDB7-0. When the WDT is running, each counter is clocked by an internal 10KHz clock. Digital I/O lines C5 and C4 are assigned as watchdog timer I/O signals when the watchdog timer is in use.

WDTEN = 1 enables the watchdog counter to run and forces DIO C5 to input and DIO C4 to output. DIO C4 is initially set to 0. Setting WDTEN = 1 also causes counters A and B to be loaded with the values in WDA15-0 and WDB7-0. Setting WDTEN = 0 stops the counters, disables the watchdog timer circuit, and returns DIO C4 and C5 to their previous configuration and values.

When running, the watchdog timer may be retriggered in two ways:

1. Writing a 1 to the WDTRIG command bit (software retrigger). If WDTRIG = 1 the remaining bits in the WDT control register are not affected.
2. If WDIEN = 1, then an edge on DIO pin C5 (hardware retrigger). WDEDGE = 0 selects rising edge, and WDEDGE = 1 selects falling edge.

A retrigger causes the following events to occur:

- Both counters A and B are reloaded with their respective values.
- DIO pin C4 is cleared to 0.

When the watchdog timer circuit is running, initially counter B is idle, and counter A counts down. When Counter A reaches 0, several events occur:

- Output pin DIO C4 goes high to provide an indicator to an external circuit of the counter timeout.
- Counter B starts to count down.
- If WDINTEN = 1, then WDINT = 1 and an interrupt will occur.

13. Mechanical Drawings

The illustrations below provide dimensions of the key connectors and features of Jasper.

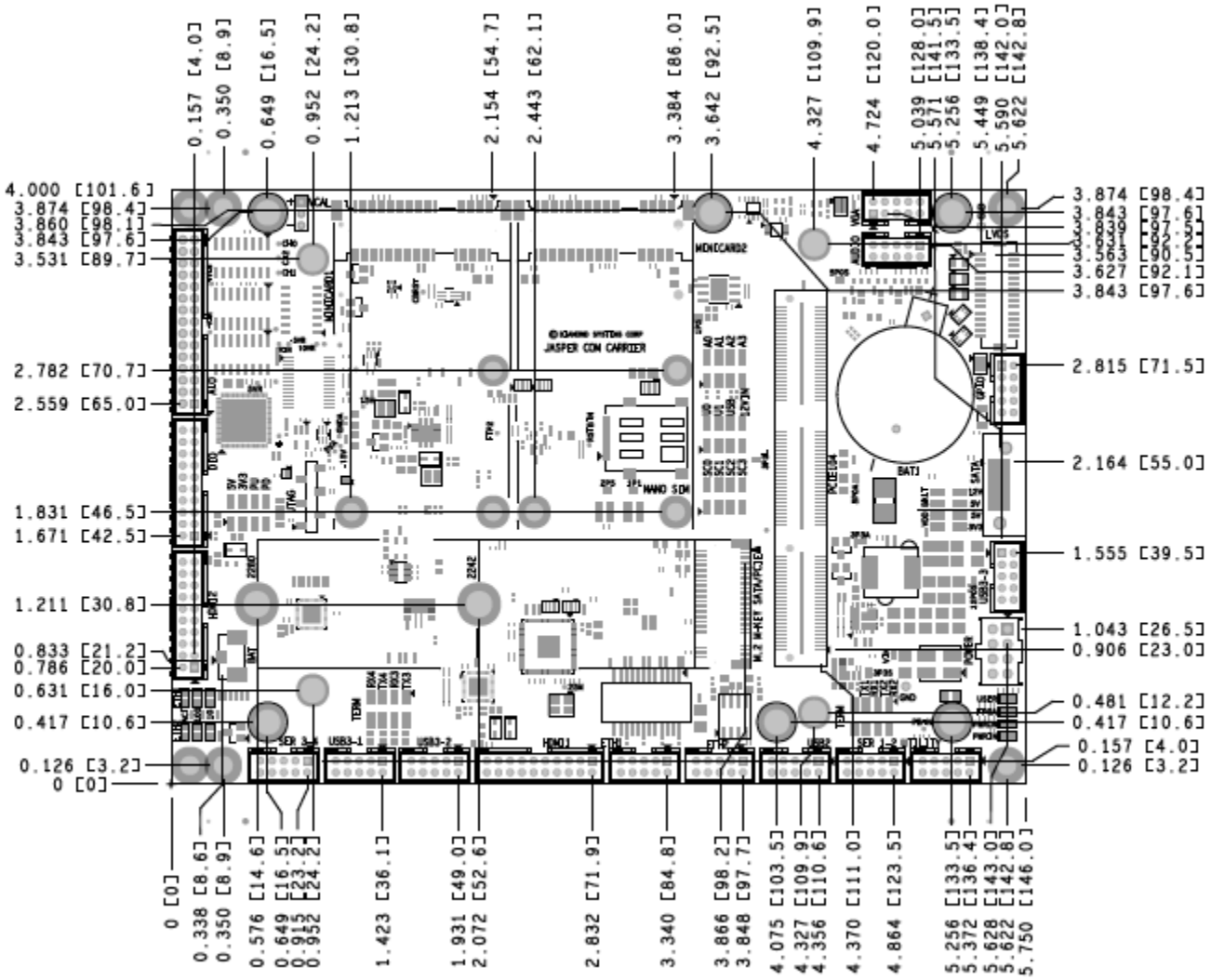


Figure 13-1: Mechanical Top View

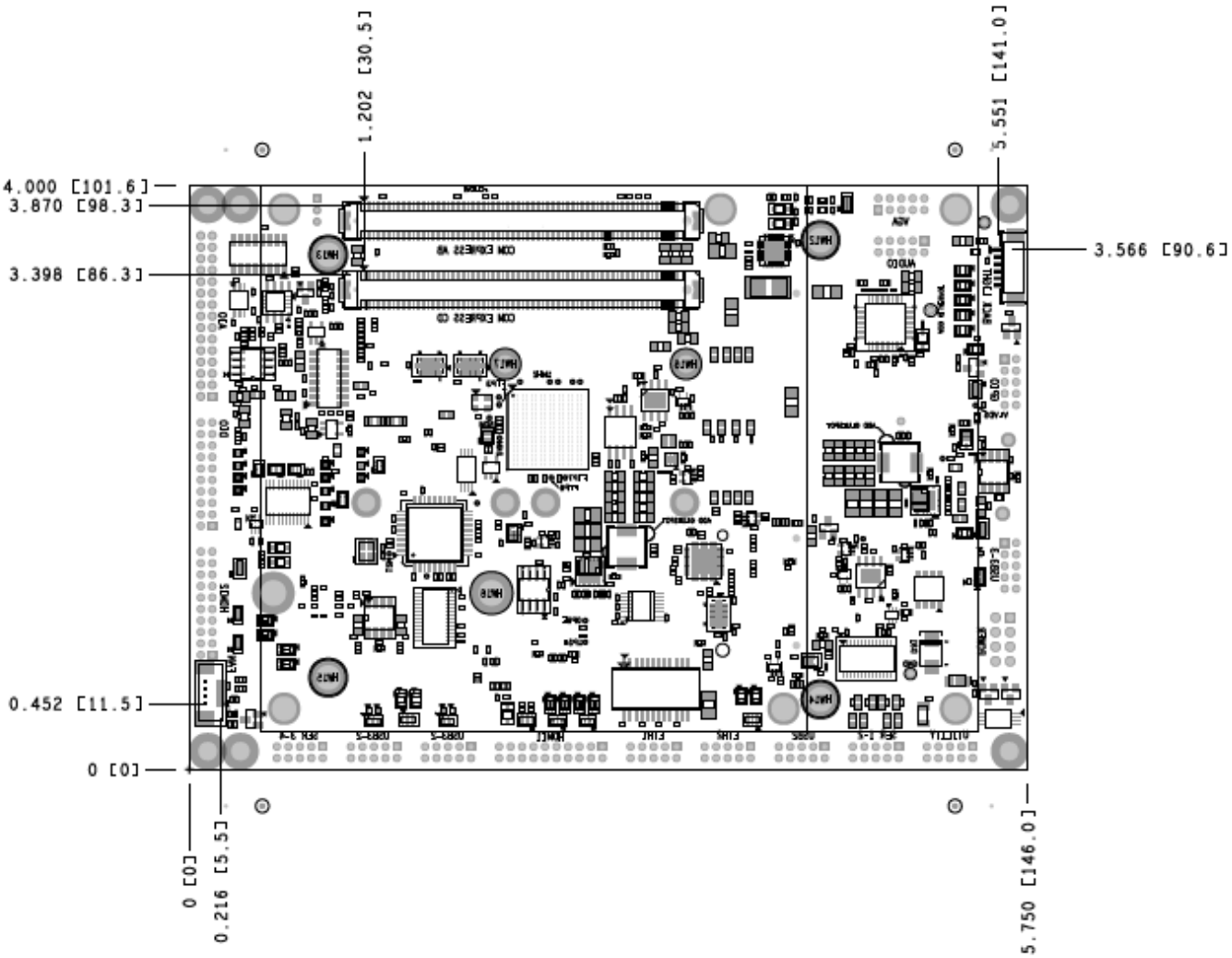


Figure 13-2: Mechanical Bottom View

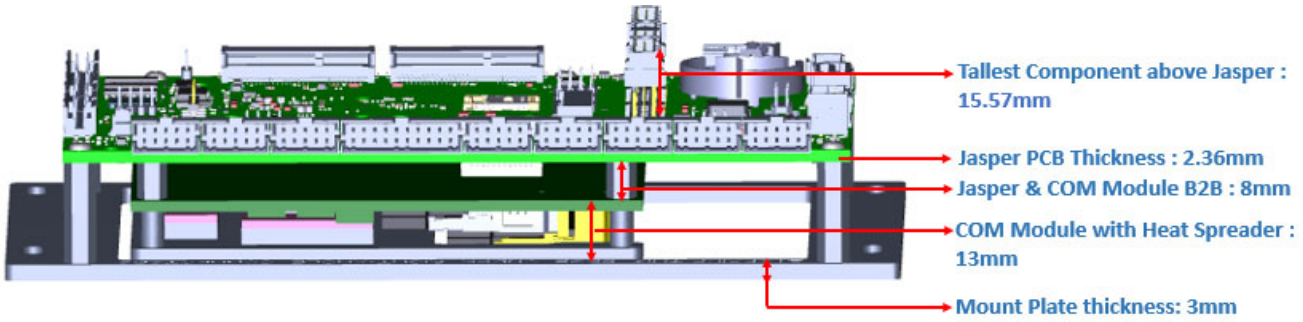


Figure 13-3: Jasper Stacking Height Details

14. Connector and Jumper Locations

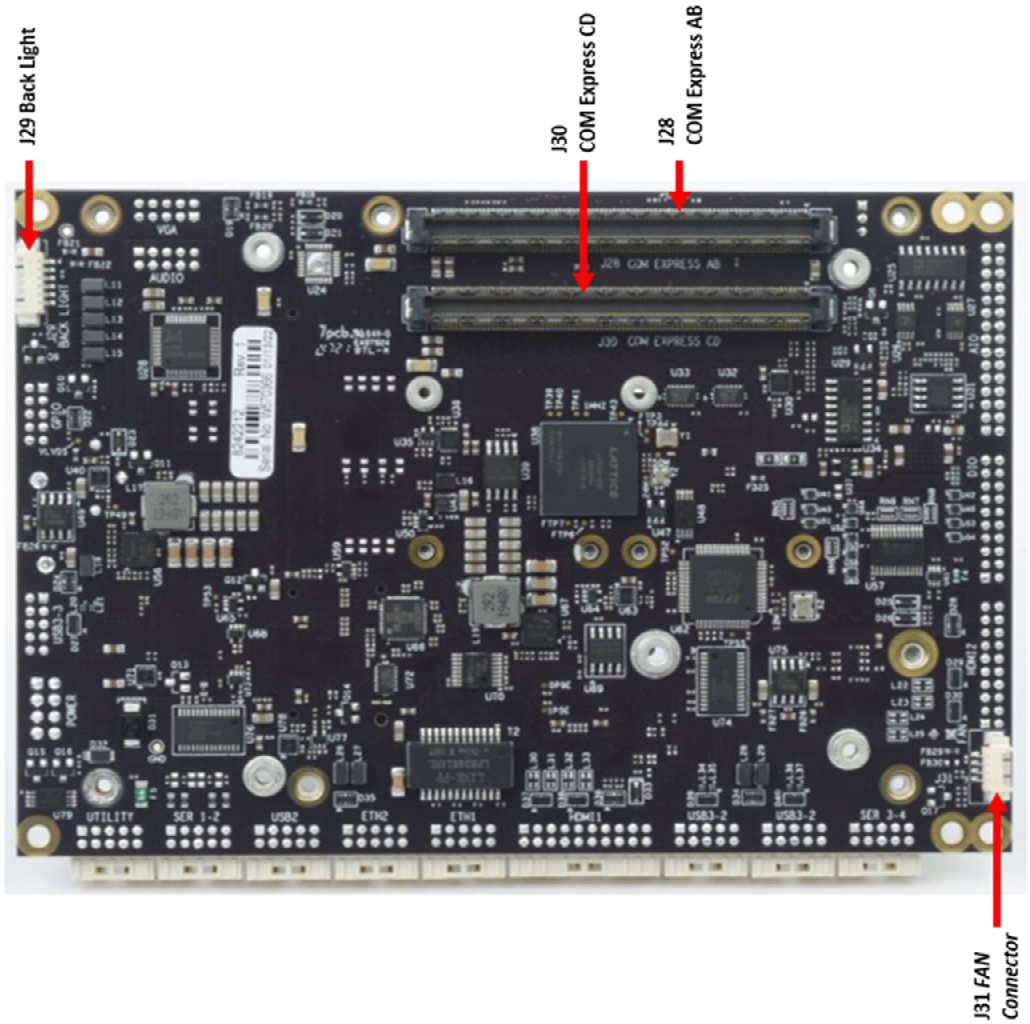


Figure 4: COM module installation side

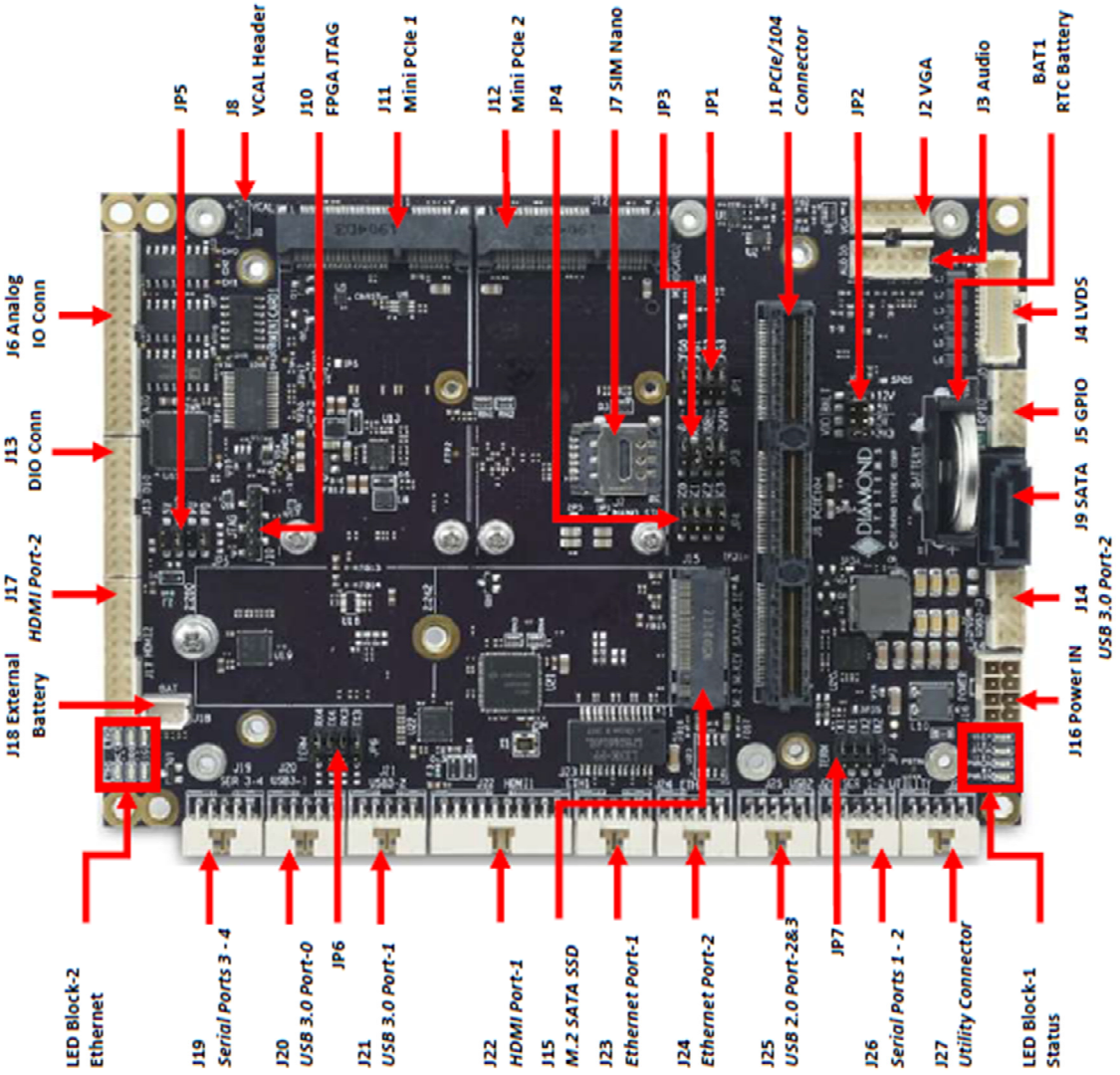


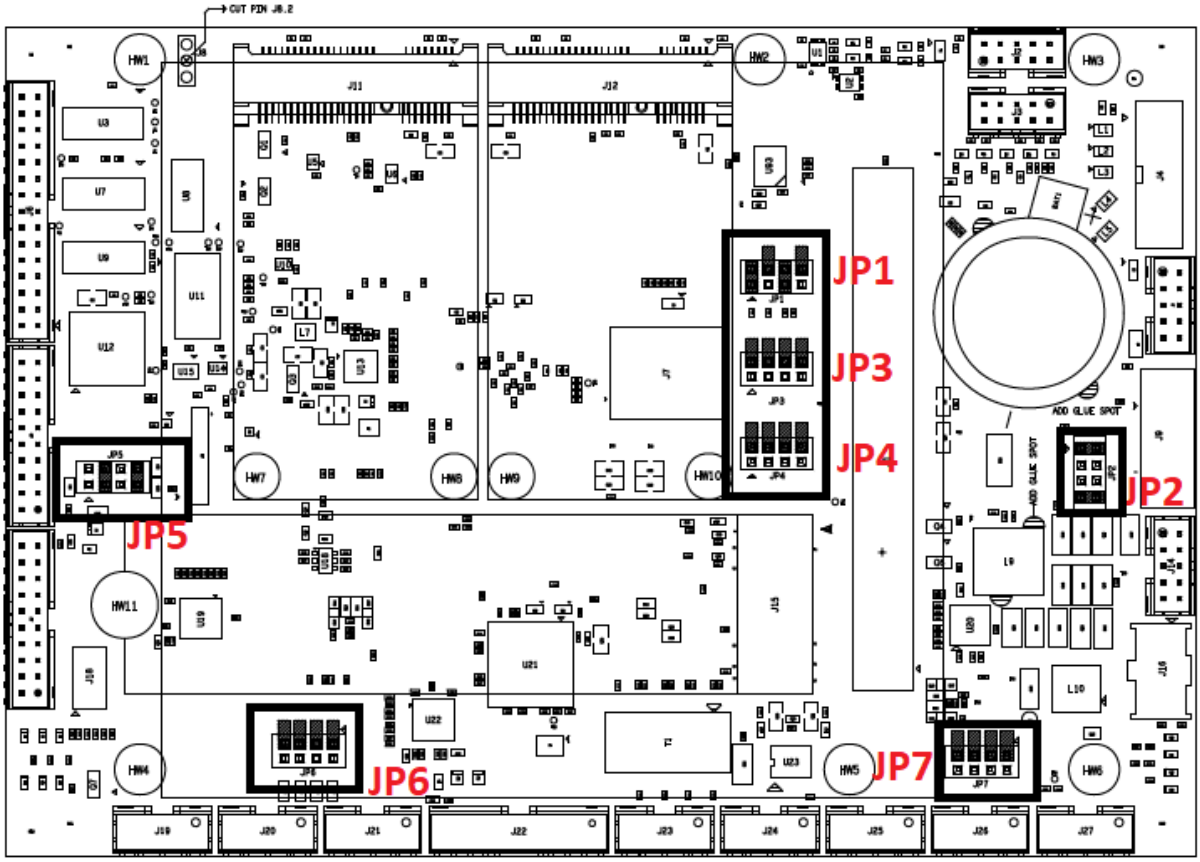
Figure 5: I/O expansion side

14.1. Jumper Selection

The Jumper blocks on the Jasper board can be configured to enable/disable or alter the default signal routing settings on the circuit, using Jumper shunts.

The following table describes the Jumper Blocks on the baseboard.

Jumper	Description
JP1	FPGA address selection
JP2	LVDS_BKLT and LVDS_VDD voltage level selection
JP3	USB TO MPCIE/PCIE/104, input voltage selection
JP4	Serial port mode selection
JP5	DIO Voltage and PU/PD selection
JP6	Serial Port 3 & 4 termination selection
JP7	Serial Port 1 & 2 termination selection



CAPTION HERE

14.1.1. Jumper Block JP1

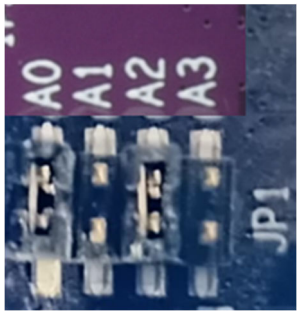
This jumper block sets the base address of the FPGA in model JSP-BB03A with data acquisition. This jumper block is not present in models without data acquisition.

Position	Function	IN (Installed)	OUT (Not Installed)
A0	FPGA Address 0	Refer below table	
A1	FPGA Address 1	Refer below table	
A2	FPGA Address 2	Refer below table	
A3	FPGA Address 3	Refer below table	
*Default Mode			

FPGA Addresses				
FPGA Address	A0	A1	A2	A3
FPGA Address - 0X100	IN	IN	IN	IN
FPGA Address - 0X120	IN	IN	IN	OUT
FPGA Address - 0X140	IN	IN	OUT	IN
FPGA Address - 0X180	IN	IN	OUT	OUT
FPGA Address - 0X200	IN	OUT	IN	IN
FPGA Address - 0X240	IN*	OUT*	IN*	OUT*
FPGA Address - 0X280	IN	OUT	OUT	IN
FPGA Address - 0X2C0	IN	OUT	OUT	OUT
FPGA Address - 0X300	OUT	IN	IN	IN
FPGA Address - 0X340	OUT	IN	IN	OUT
FPGA Address - 0X380	OUT	IN	OUT	IN
FPGA Address - 0X3C0	OUT	IN	OUT	OUT
FPGA Address - 0X400	OUT	OUT	IN	IN
FPGA Address - Reserved	OUT	OUT	IN	OUT
FPGA Address - Reserved	OUT	OUT	OUT	IN
FPGA Address - Reserved	OUT	OUT	OUT	OUT
*Default setting				

Note: 1. Base address must be selected based on addresses available on the COM module used with Jasper. Check the COM user manual for available addresses.

Following image shows the jumper configuration for FPGA address 0x240*

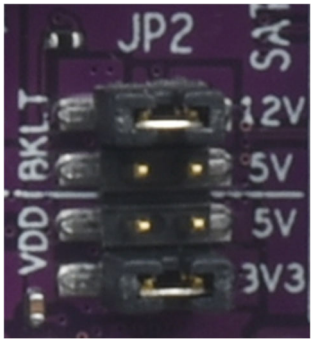


14.1.2. Jumper Block JP2

JP2 Jumpers are provided to select the voltage level of the LVDS display and backlight.

Position	Function	IN (Installed)	OUT (Not Installed)
12V	LCD Backlight Voltage	12V*	-
5V	LCD Backlight Voltage	5V	-
5V	LCD VDD Voltage	5V	-
3V3	LCD VDD Voltage	3.3V*	-
*Default Mode			

Following image shows the jumpers are configured for LCD Back light voltage of 12V and LCD VDD voltage of 3.3V.

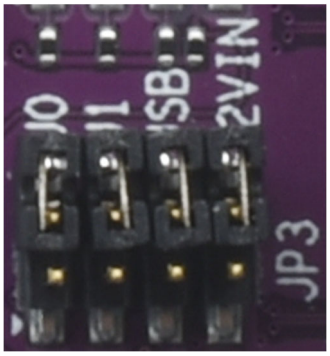


14.1.3. Jumper Block JP3

JP3 Jumpers are provided to select the configuration pins of the FPGA, USB interface and Power IN option. USB interface from COMe Type AB connector is multiplex to mPCIe and PCIe/104 connector. Board can be powered with 15V-36V wide input or 12V fixed supply.

Position	Function	IN (Installed)	OUT (Not Installed)
U0	FPGA Config 0	TBD	TBD*
U1	FPGA Config 1	TBD	TBD*
USB	USB SEL	Minicard	PCIe104*
12VIN	Wide Input SEL	12V Fixed	Wide Input* (15-36V)
*Default Mode			

Following image shows all jumpers are “OUT”. Which selects PCIe104 and Wide input voltage.



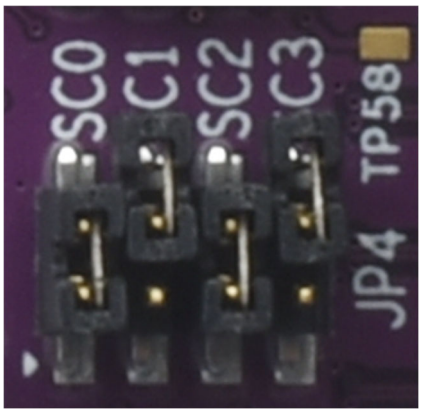
14.1.4. Jumper Block JP4

JP4 Jumpers are provided to select the mode of serial ports 1, 2, 3 & 4. SC0 and SC1 jumpers are used to select mode for serial ports 1 & 2 and SC2 and SC3 jumpers are used to select mode for serial ports 3 & 4.

Position	Port	RS232	RS485	RS422	Internal Loop
SC0	1&2	IN*	OUT	OUT	IN
SC1	1&2	OUT*	IN	OUT	IN
SC2	3&4	IN*	OUT	OUT	IN
SC3	3&4	OUT*	IN	OUT	IN
*Default setting					

Applicable only for JSP-BB02D model. JP4 Jumper is software overridden by FGPA for JSP-BB03A model.

Following image shows jumper configuration in RS232 mode.



14.1.5. Jumper Block JP5

JP5 Jumpers are provided to select the voltage level and Pullup/pull down configuration of the DIO on models with data acquisition. By default, the DIOs are 3.3V and pulled down.

Position	Function	IN (Installed)	OUT (Not Installed)
5V	DIO Voltage Level	5V	-
3V3	DIO Voltage Level	3.3V*	-
PU	DIO Pull Up Enable	Enabled	Disabled
PD	DIO Pull Down Enable	Enabled*	Disabled
*Default setting			

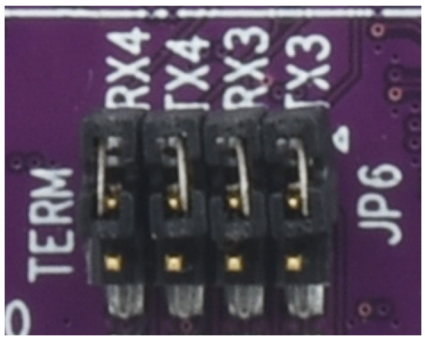
Following image shows the jumper configuration to select 3.3V and PD enable.

14.1.6. Jumper Block JP6

JP6 Jumpers Configuration are provided enable and disable the termination of serial ports3-4. This feature is not available in model JSP-BB01D.

Position	Function	IN (Installed)	OUT (Not Installed)
TX3	Serial Port3 TX Termination	Enabled	Disabled*
RX3	Serial Port3 RX Termination	Enabled	Disabled*
TX4	Serial Port4 TX Termination	Enabled	Disabled*
RX4	Serial Port4 RX Termination	Enabled	Disabled*
*Default setting			

Following image shows the jumper configuration to disable all four terminations by keeping all jumpers OUT.



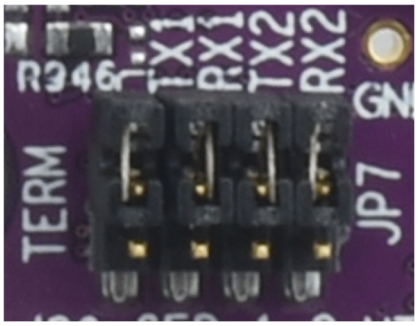
14.1.7. Jumper Block JP7

JP7 Jumpers Configuration are provided enable and disable the termination of serial ports1-2. This jumper block is not available in model JSP-BB01D. On that model, the serial ports are fixed in RS-232 configuration.

Position	Function	IN (Installed)	OUT (Not Installed)
TX1	Serial Port1 TX Termination	Enabled	Disabled*

RX1	Serial Port1 RX Termination	Enabled	Disabled*
TX2	Serial Port2 TX Termination	Enabled	Disabled*
RX2	Serial Port2 RX Termination	Enabled	Disabled*
*Default setting			

Following image shows the jumper configuration where all terminations are disabled by keeping all jumpers OUT.



15. Connector Pinouts

15.1. Analog I/O (J6)

The VIO pins on the analog and digital I/O connectors are tied together on the board and provide access to jumper-selectable 3.3V / 5V system voltage rail through a polyswitch resettable fuse. The fuse is rated for ~100mA maximum sustained current.

VIO (fused)	**A01**	**B01**	Digital Ground
DIO C3	**A02**	**B02**	DIO C4
DIO C1	**A03**	**B03**	DIO C2
Analog Ground	**A04**	**B04**	DIO C0
Aout 2	**A05**	**B05**	Aout 3
Aout 0	**A06**	**B06**	Aout 1
Analog Ground	**A07**	**B07**	Analog Ground
Ain 7	**A08**	**B08**	Ain 15
Ain 6	**A09**	**B09**	Ain 14
Ain 5	**A10**	**B10**	Ain 13
Ain 4	**A11**	**B11**	Ain 12
Ain 3	**A12**	**B12**	Ain 11
Ain 2	**A13**	**B13**	Ain 10
Ain 1	**A14**	**B14**	Ain 9
Ain 0	**A15**	**B15**	Ain 8

Connector PN: 98414-G06-30LF

Connector Type: latching 2x15 2mm pitch vertical shrouded pin header

Mating Cable PN: 6980612

15.2. Audio (J3)

This connector provides the audio signals.

LineOut-L	**A01**	**B01**	LineOut-R
GND_Audio	**A02**	**B02**	GND_Audio
LineIn-L	**A03**	**B03**	LineIn-R
GND_Audio	**A04**	**B04**	GND_Audio
NC	**A05**	**B05**	MIC_IN

Connector PN: 98414-G06-10LF **Connector Type:** latching 2x5 2mm pitch vertical shrouded pin header. **Mating Cable PN:** 6980608	

15.3. Battery (J18)

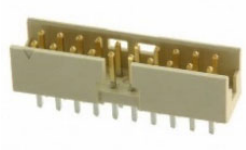
An external battery may be connected to support real-time clock and BIOS custom settings.

1	Battery V+
2	Ground

Connector PN: 053398-0271 **Connector Type:** 2 position 1.25 mm pitch vertical SMD header **Mating Cable PN:** DSC no. 4713001 (CR2032 Battery with Wire Leads) DSC no. 6980529 (Battery cable with free wires)	

15.4. Digital I/O (J13)

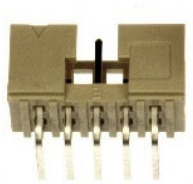
VIO (fused)	**A01**	**B01**	DIO A0
DIO A1	**A02**	**B02**	DIO A2
DIO A3	**A03**	**B03**	DIO A4
DIO A5	**A04**	**B04**	DIO A6
DIO A7	**A05**	**B05**	DIO B0
DIO B1	**A06**	**B06**	DIO B2
DIO B3	**A07**	**B07**	DIO B4
DIO B5	**A08**	**B08**	DIO B6
DIO B7	**A09**	**B09**	DIO C5
Ground	**A10**	**B10**	Ground

Connector PN: 98414-F06-20ULF **Connector Type:** latching 2x10 2mm pitch vertical shrouded pin header **Mating Cable PN:** 6980611	

15.5. Ethernet (J23 & J24)

There are two identical on-board connectors for 10/100/1000 BASE T Ethernet.

Chassis Gnd	**A01**	**B01**	NC
DA+	**A02**	**B02**	DA-
DB+	**A03**	**B03**	DB-
DC+	**A04**	**B04**	DC-
DD+	**A05**	**B05**	DD-

Connector PN: 98464-G61-10ULF **Connector Type:** latching 2x5 2mm pitch RA shrouded pin header. **Mating Cable PN:** 6980604	

15.6. Fan Connector (J31)

An external fan can be connected as a thermal solution for effective heat dissipation where conduction cooling is not possible.

1	Fan PWM
2	Fan Tach
3	Fan PWR (5V/12V)
4	GND

Connector PN: Molex 0532610471 **Connector Type:** 4 pin Right Angle Surface Mount shrouded pin header **Recommended Fan PN:** ASB0305HP-00CP4	

15.7. GPIO Connector (J5)

The GPIO connector provides access to 4 GPO and 4 GPI along with fused 3.3V power that can be used for powering customer auxiliary circuitry. GPI3 is muxed with the TPM IRQ and is available as general purpose input to the COM module by default.

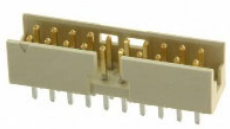
GPI0	**A01**	**B01**	GPO0
GPI1	**A02**	**B02**	GPO1
GPI2	**A03**	**B03**	GPO2
GPI3	**A04**	**B04**	GPO3
3.3V Fused 0.5A	**A05**	**B05**	GND

Connector PN: 98414-G06-10LF
Connector Type: latching 2x5 2mm pitch vertical shrouded pin header
Mating Cable PN: 6980609

15.8. HDMI (J17)

Data 2+	**A01**	**B01**	Ground
Data 2-	**A02**	**B02**	Data 1+
Ground	**A03**	**B03**	Data 1-
Data 0+	**A04**	**B04**	Ground
Data 0-	**A05**	**B05**	Clock+
Ground	**A06**	**B06**	Clock-
CEC	**A07**	**B07**	Reserved
DDC Clock	**A08**	**B08**	DDC Data
Ground	**A09**	**B09**	+5V
Hot Plug Detect	**A10**	**B10**	Chassis ground

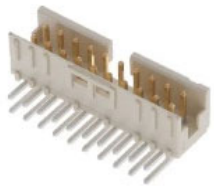
Connector PN: 98414-F06-20ULF
Connector Type: latching 2x10 2mm pitch vertical shrouded pin header on the left edge of board.
Mating Cable PN: 6980605



15.9. HDMI (J22)

The board supports 2 HDMI ports. HDMI signals come through a level translator IC from COM module over DDI lanes.

Data 2+	**A01**	**B01**	Ground
Data 2-	**A02**	**B02**	Data 1+
Ground	**A03**	**B03**	Data 1-
Data 0+	**A04**	**B04**	Ground
Data 0-	**A05**	**B05**	Clock+
Ground	**A06**	**B06**	Clock-
CEC	**A07**	**B07**	Reserved
DDC Clock	**A08**	**B08**	DDC Data
Ground	**A09**	**B09**	+5V
Hot Plug Detect	**A10**	**B10**	Chassis ground

Connector PN: 98464-G61-20ULF **Connector Type:** latching 2x10 2mm pitch RA shrouded pin header on the front edge of board **Mating Cable PN:** 6980605	

15.10. LCD Backlight (J29)

The brightness control for the LCD backlight has a weak pull-down resistor to ensure maximum brightness when it is not connected externally. This signal may be controlled by a PWM pin on the COM module. A jumper selects the source of the brightness signal to this pin.

1	Power +5V/+12V, jumper selectable
2	Power (same as pin 1)
3	Ground
4	Ground
5	Enable (GPIO output), 0 = off, open circuit = on
6	Brightness, 0-3.3VDC variable; 0V = max, 3.3V = min

Connector PN: JS-1147H-06 **Connector Type:** 1x6 1.25mm pitch SMD RA header **Mating Cable:** Custom depending on the target display.	

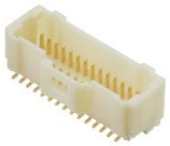
15.11. LVDS (J4)

The LCD panel power is jumper-selectable for 3.3V (default) or 5V.

VDD 5V/3.3V	**1**	**2**	VDD 5V/3.3V
VDD 5V/3.3V	**3**	**4**	VDD 5V/3.3V
CLK+ Odd	**5**	**6**	CLK+ Even
CLK- Odd	**7**	**8**	CLK-Even
Ground	**9**	**10**	Ground
D0+ Odd	**11**	**12**	D0+ Even
D0- Odd	**13**	**14**	D0- Even
D1+ Odd	**15**	**16**	D1+ Even
D1- Odd	**17**	**18**	D1- Even
D2+ Odd	**19**	**20**	D2+ Even
D2- Odd	**21**	**22**	D2- Even
D3+ Odd	**23**	**24**	D3+ Even
D3- Odd	**25**	**26**	D3- Even

Ground	27	28	Ground
DDC CLK	29	30	DDC DATA

Connector PN: 5011903027
Connector Type: 1mm pitch vertical shrouded pin header
Mating Cable: Custom depending on the target display

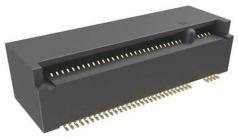


15.12. M.2 Socket (J15)

M.2 2280/2242 supports SATA / PCIe using a high-speed mux. All TX/RX signals are with respect to the host. TX on the socket drives RX on the installed module, and RX on the socket is driven by TX on the installed module. The mounting standoffs of the module installation site is not connected to ground.

Gnd	1	2	+3.3V
Gnd	3	4	+3.3V
	5	6	MEM_ERS_2
	7	8	MEM_ERS_1
	9	10	
	11	12	+3.3V
	13	14	+3.3V
	15	16	+3.3V
	17	18	+3.3V
	19	20	
Gnd	21	22	
	23	24	
	25	26	
Gnd	27	28	
	29	30	
	31	32	
Gnd	33	34	
	35	36	
	37	38	
Gnd	39	40	
SATA_RX+/ PCIe RX-	41	42	
SATA_RX-/PCIe RX+	43	44	
Gnd	45	46	
SATA_TX-/PCIe TX-	47	48	
SATA_TX+/PCIe TX+	49	50	PERST#
Gnd	51	52	PCIe CLKREQ#

PCIe REFCLK-	53	54	PCIe WAKE#
PCIe REFCLK+	55	56	
Gnd	57	58	
	KEY		
	67	68	
	69	70	+3.3V
Gnd	71	72	+3.3V
Gnd	73	74	+3.3V
Gnd	75		

Connector PN: 10128798-005RLF **Connector Type:** 75 Position Female Connector M.2 (NGFF) Mini Card	

15.13. PCIe Mini Card (J11 & J12)

Minicard supports SATA / PCIe using high-speed mux. All TX/RX signals are with respect to the host. TX on the socket drives RX on the installed module, and RX on the socket is driven by TX on the installed module. The mounting standoffs of the module installation site are not connected to ground.

PCIe WAKE#	1	2	+3.3V
	3	4	Gnd
	5	6	+1.5V
PCIe CLKREQ#	7	8	
Gnd	9	10	
PCIe CLK-	11	12	
PCIe 1 Clk+	13	14	
Gnd	15	16	
	KEY		
	17	18	Gnd
	19	20	
Gnd	21	22	PCIe Reset-
PCIe RX-/SATA RX+	23	24	+3.3V
PCIe RX+/SATA RX-	25	26	Gnd
Gnd	27	28	+1.5V
Gnd	29	30	SMB Clk
PCIe TX-/SATA TX-	31	32	SMB Data
PCIe TX+/SATA TX+	33	34	Gnd
Gnd	35	36	USB D-

Gnd	37	38	USB D+
+3.3V	39	40	Gnd
+3.3V	41	42	
Ground	43	44	
	45	46	
	47	48	+1.5V
	49	50	Gnd
	51	52	+3.3V

Connector PN: 1759547-1
Connector Type: 52 Position Female Connector PCI Express Mini Card

15.14. Power In (J16)

A 2x4 latching pin header is used for power input.

VIN = 12V or 15V to 36V

GND	1	5	VIN
GND	2	6	VIN
GND	3	7	VIN
GND	4	8	VIN

Connector PN: IPL1-104-01-L-D-K
Connector Type: 2.54mm pitch 2x4 box header TH vertical
Mating Cable PN: 6980512

15.15. SATA (J9)

The SATA connector is an industry-standard vertical connector. This connector does not support the Pin 7 Vcc option for an installed SATA DOM.

1	Ground
2	Transmit +
3	Transmit -
4	Ground
5	Receive -

6	Receive +
7	Ground

Connector PN: 0678005025 **Connector Type:** 7 Position SATA Header, Shrouded Connector **Mating Cable PN:** 6989101	

15.16. Serial ports (J26)

The COM express carrier board supports 4 serial ports available at 2 headers in full feature variant and only 2 RS232 ports at one of the connectors in low-cost variant.

Each connector supports 2 serial ports. Pinouts are as follows depending on the mode of the transceiver (RS232/ RS422/ RS485).

RS-232:

TX1	**A01**	**B01**	RTS1
RX1	**A02**	**B02**	CTS1
GND	**A03**	**B03**	GND
TX2	**A04**	**B04**	RTS2
RX2	**A05**	**B05**	CTS2

RS-422:

TX1+	**A01**	**B01**	TX1-
RX1+	**A02**	**B02**	RX1-
GND	**A03**	**B03**	GND
TX2+	**A04**	**B04**	TX2-
RX2+	**A05**	**B05**	RX2-

RS-485:

TX1/RX1+	**A01**	**B01**	TX1/RX1-
NC	**A02**	**B02**	NC
GND	**A03**	**B03**	GND
TX2/RX2+	**A04**	**B04**	TX2/RX2-
NC	**A05**	**B05**	NC

15.17. Serial ports (J19)

RS-232

TX3	**A01**	**B01**	RTS3
RX3	**A02**	**B02**	CTS3
Ground	**A03**	**B03**	Ground
TX4	**A04**	**B04**	RTS4
RX4	**A05**	**B05**	CTS4

RS-422

TX3+	**A01**	**B01**	TX3-
RX3+	**A02**	**B02**	RX3-
Ground	**A03**	**B03**	Ground
TX4+	**A04**	**B04**	TX4-
RX4+	**A05**	**B05**	RX4-

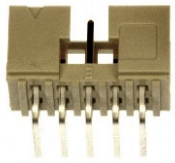
RS-485

TX3/RX3+	**A01**	**B01**	TX3/RX3-
NC	**A02**	**B02**	NC
Ground	**A03**	**B03**	Ground
TX4/RX4+	**A04**	**B04**	TX4/RX4-
NC	**A05**	**B05**	NC

Connector PN: 98464-G61-10ULF

Connector Type: latching 2x5 2mm pitch right angle shrouded pin header

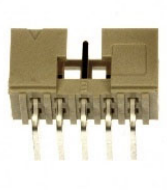
Mating Cable PN: 6980601



15.18. USB 2.0 Ports (J25)

The Carrier board supports 2 USB2.0 ports on a 2x5 connector. The pinout for the connector is as shown below:

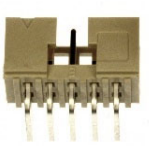
NC	**A01**	**B01**	Shield
USB1 Pwr-	**A02**	**B02**	USB0 Pwr-
USB1 Data+	**A03**	**B03**	USB0 Data+
USB1 Data-	**A04**	**B04**	USB0 Data-
USB1 Pwr+	**A05**	**B05**	USB0 Pwr+

Connector PN: 98464-G61-10ULF **Connector Type:** latching 2x5 2mm pitch RA shrouded pin header **Mating Cable PN:** 6980602	

15.19. USB 3.0 Ports (J20, J21)

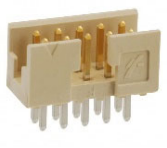
The Carrier board supports 3 USB3.0 ports on identical on-board 2x5 connectors. The connector supports backward compatibility to USB2.0. Pinout of the same is shown below:

USB_SSRX0-	**A01**	**B01**	Shield
USB_SSRX0+	**A02**	**B02**	USB Pwr-
USB Pwr-	**A03**	**B03**	USB2 D+
USB_SSTX0-	**A04**	**B04**	USB2 D-
USB_SSTX0+	**A05**	**B05**	USB Pwr+

Connector PN: 98464-G61-10ULF **Connector Type:** latching 2x5 2mm pitch RA shrouded pin header on the front edge of the board. **Mating Cable PN:** 6980603	

15.20. USB 3.0 Ports (J14)

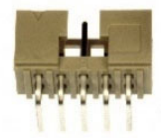
USB_SSRX0-	**A01**	**B01**	Shield
USB_SSRX0+	**A02**	**B02**	USB Pwr-
USB Pwr-	**A03**	**B03**	USB2 D+
USB_SSTX0-	**A04**	**B04**	USB2 D-
USB_SSTX0+	**A05**	**B05**	USB Pwr+

Connector PN: 98414-G06-10LF **Connector Type:** latching 2x5 2mm pitch vertical shrouded pin header on the right edge of board. **Mating Cable PN:** 6980603	

15.21. Utility (J27)

The utility connector provides access to power button, reset signal, I2C and RTC power. It provides fused 3.3V power that can be used for powering customer auxiliary circuitry.

M_2_MEM_ERS_GPIO	**A01**	**B01**	I2C Clock
Ground	**A02**	**B02**	I2C Data
Ground	**A03**	**B03**	Power Button
V_3P3_RTC	**A04**	**B04**	Ground
3.3V Fused 0.5A	**A05**	**B05**	Reset

Connector PN: 98464-G61-10ULF **Connector Type:** latching 2x5 2mm pitch right angle shrouded pin header **Mating Cable PN:** 6980609	

15.22. VGA (J2)

VGA availability is dependent on the installed COM.

VGA_RED	**A01**	**B01**	GND
VGA_GREEN	**A02**	**B02**	NC
VGA_BLUE	**A03**	**B03**	GND
VGA_HSYNC	**A04**	**B04**	VGA_DDC_DATA
VGA_VSYNC	**A05**	**B05**	VGA_DDC_CLK

Connector PN: FCI 98414-G06-10LF **Connector Type:** latching 2x5 2mm pitch vertical shrouded pin header **Mating Cable PN:** 6981084	

16. I/O Connector List & Mating Cables

The following table provides a summary of the I/O connectors on the board.

Function	Manufacturer	Part no.	Description	DSC Mating Cable
Power in	Samtec	IPL1-104-01-L-D-K	2x4 latching box header TH vertical .1" pitch, long PCB pins	6980512
USB 2.0	Amphenol	98464-G61-10ULF	2x5 2mm pitch latching RA TH header	6980602
USB 3.0 qty 2	Amphenol	98464-G61-10ULF	2x5 2mm pitch latching RA TH header	6980603
USB 3.0 qty 1	Amphenol	98414-G06-10LF	2x5 2mm pitch latching vertical TH header	6980603
Ethernet qty 2	Amphenol	98464-G61-10ULF	2x5 2mm pitch latching RA TH header	6980604
Serial Ports qty 2	Amphenol	98464-G61-10ULF	2x5 2mm pitch latching RA TH header	6980601
LVDS	Molex	5011903027	2x15 1mm pitch vertical SMT shrouded header	Custom
HDMI qty 1	Amphenol	98464-G61-20ULF	2x10 2mm pitch latching RA TH header	6980605
HDMI qty 1	Amphenol	98414-F06-20ULF	2x10 2mm pitch latching vertical TH header	6980605
Backlight	Molex	JS-1147H-06	1x6 1.25mm pitch SMD RA header	Custom
External battery	Molex	0533980271	2 position 1.25mm pitch vertical SMD header	4713001 or 6980529
Analog I/O	Amphenol	98414-G06-30LF	30 Pos 1.5mm Pitch SMT vertical Latching	6980612
Digital I/O	Amphenol	98414-F06-20ULF	20 Pos 1.25mm Pitch SMT vertical Latching	6980611
Audio	Amphenol	98414-G06-10LF	2x5 2mm pitch latching vertical TH header	6980608
VGA	Amphenol	98414-G06-10LF	2x5 2mm pitch latching vertical TH header	6981084
Utility	Amphenol	98464-G61-10ULF	2x5 2mm pitch latching RA TH header	6980609
GPIO	Amphenol	98414-G06-10LF	2x5 2mm pitch latching vertical TH header	6980609
FAN	Molex	0532610471	1x4 1.25mm pitch SMD vertical header	NA
PCIe104	Samtec	ASP-142781-03	156 Pos Top Mount	NA
M.2	Amphenol	10128798-005RLF	Connector Female 67position 0.020 pitch	NA
SATA	Molex	0678005025	Connector header 7 position vertical TH	6989101
PCIe Minicard	TE	1759547-1	52-pin Minicard, full size, with PCB mount threaded spacers	NA
COM Express Compact	Foxconn	QT002206-4131-3H	220 Position Connector Plug, SMT, Outer Shroud Contacts Surface Mount Gold	NA

* Representative part; other manufacturers / part numbers are also acceptable; confirm selection with DSC

17. Jasper vs COM Module Interface Comparison List

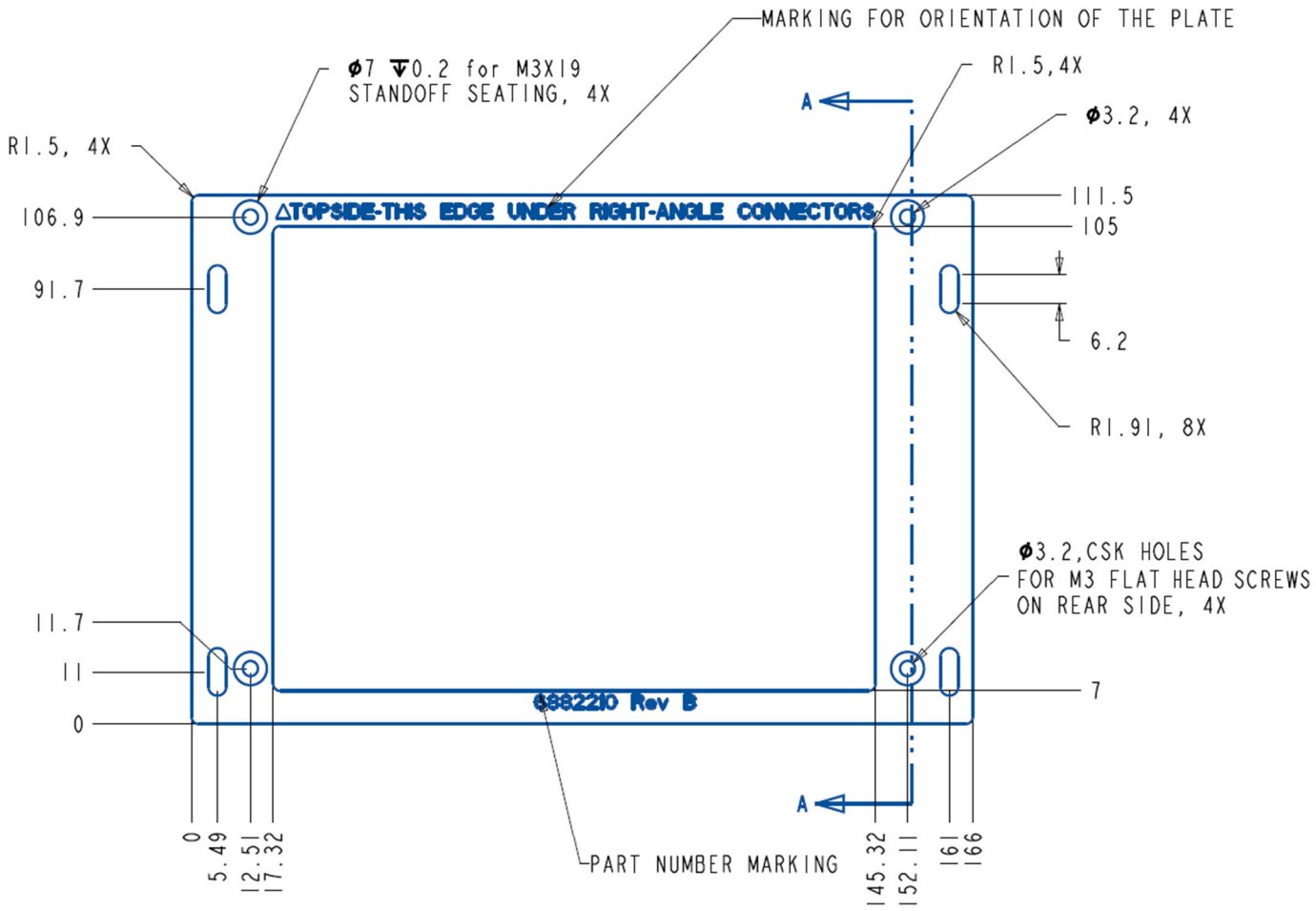
Interfaces as in COM Specification	Available on Carrier Board	Available on SBC Assembly	
	Models JSP-BBxxx	Winsystems COMET6-110	Arbor EmETXe-i92U1
PCIe Port0 on AB	Minicard 1 SATA & PCIe Muxed	Yes	Yes
PCIe Port1 on AB	Minicard 2 SATA & PCIe Muxed	Yes	Yes
PCIe Port2 on AB	PCIe104 Bank 1 Lane_0	Yes	Yes
PCIe Port3 on AB	I210 Ethernet controller	Yes	Yes
PCIe Port4 on AB	PCIe104 Bank 1 Lane_1	Yes	Yes
PCIe Port5 on AB	PCIe104 Bank 1 Lane_2	No	Yes
PCIe Port6 on CD	PCIe104 Bank 1 Lane_3	No	Yes
PCIe Port7 on CD	M.2 2242/2280 SATA & PCIe supported	No PCIe; SATA only	Yes, PCIe and SATA
PEG x16 on CD	PCIe104 Bank 2 & 3	No (Only 4 Lanes available; Configurable as 4 x1(default) or 2 x1 + 1 x2 or 1x4)	No (Only 4 Lanes available; fixed configuration 1x PCIex4)
LVDS on AB	LVDS	Yes (Optional)	Yes
DDI0 on CD	HDMI 1	Yes	Yes
DDI1 on CD	HDMI 2	Yes	Yes
DDI2 on CD	Not Supported	NA	NA
VGA	VGA	Yes (Optional)	Yes
USB2.0 Port0	USB3.0 Header-1	Yes	Yes
USB2.0 Port1	USB3.0 Header-2	Yes	Yes
USB2.0 Port2	USB2.0 Header-1	Yes	Yes
USB2.0 Port3	USB2.0 Header-1	Yes	Yes
USB2.0 Port4	USB to UART	Yes	Yes
USB2.0 Port5	Minicard 2	Yes	Yes
USB2.0 Port6	Minicard 1 / PCIe104 Bank 1 Port_0	Yes	Yes
USB2.0 Port7	USB3.0 Header-3	Yes	Yes
USB3.0 Port0	USB3.0 Header-1	Yes	Yes
USB3.0 Port1	USB3.0 Header-2	Yes	Yes
USB3.0 Port2	USB3.0 Header- 3	Yes	Yes
USB3.0 Port3	Not Supported	NA	NA

Interfaces as in COM Specification	Available on Carrier Board	Available on SBC Assembly	
	Models JSP-BBxxx	**Winsystems COMET6-110**	**Arbor EmETXe-i92U1**
SATA Port0	M.2 2242/2280 SATA & PCIe Muxed	Yes	Yes
SATA Port1	7 Pin SATA	Yes	Yes
SATA Port2	Minicard 1 SATA & PCIe Muxed	No	No
SATA Port3	Minicard 2 SATA & PCIe Muxed	No	No
HD Audio	Audio	Yes	Yes
LPC	Data acquisition circuit Model JSP-BB03A only	Yes	Yes
GbE Lan	GbE	Yes (2.5G)	Yes (1G)
UART 0	1x RS-232	Yes	Yes
UART 1	1x RS-232	Yes	Yes
4x GPI & 4x GPO	4x GPI, 4x GPO	Yes	Yes

18. Mounting Plate

Jasper includes an aluminum mounting plate that enables convenient installation into an enclosure. The board assembly is mounted on the plate using M3 19mm long standoffs. Slots in the corners allow flexibility in the installed position. This is useful for installations where the front row of I/O connectors is directly mated to an I/O board.

The plate contains a cutout in the center to fit the standard heat spreader provided by the COM vendor. The COM Express standard defines a standard height for all heat spreaders, enabling the Jasper mounting plate to be used with any compliant COM heat spreader. The mounting pate is 0.9mm taller than the standard heat spreader height to allow for installing a 1mm thick thermal pad between the heat spreader and the enclosure surface for improved thermal conductivity. All standard models of Jasper include thermal pads for use in this manner.



CAPTION HERE

19. Getting Started

JetBox-Jackson is a compact, ready-to-deploy Nvidia Jetson AI computing platform. Below steps help you to create practical AI applications, impressive AI robots, and more.

19.1. Powering Up System

Refer to the below section to power on the JetBox-Jackson system. The system is pre-programmed and ready to run. Attach KB / MS / display / power to start the system.

Required Accessories

- Any carrier board which has M.2 M-Key NVMe slot and able to boot without M.2 M-Key NVMe
- Host PC installed with Ubuntu 20.4 x86_64, Kernel version: 5.15.0-52 or above
- USB A to USB A cable
- M.2 Key M 2280 NVMe PCIe SSD
- Jackson board assembled with Orin NX/Nano module
- Jackson BSP released files

Bringing up JetBox-Jackson

JetBox-Jackson is shipped to our customers ready to work out of the box. A 12V DC adapter is included with the JetBox-Jackson. The JetBox module, included with the JetBox Jackson, is flashed with the latest BSP. However, it is highly recommended to check the Diamond System Corp website for any updated BSPs at https://www.diamondsystems.com/products/jackson.

To get started with JetBox-Jackson, a minimum of USB keyboard, USB mouse and an HDMI monitor are required. Refer to the reference set up image provided below:

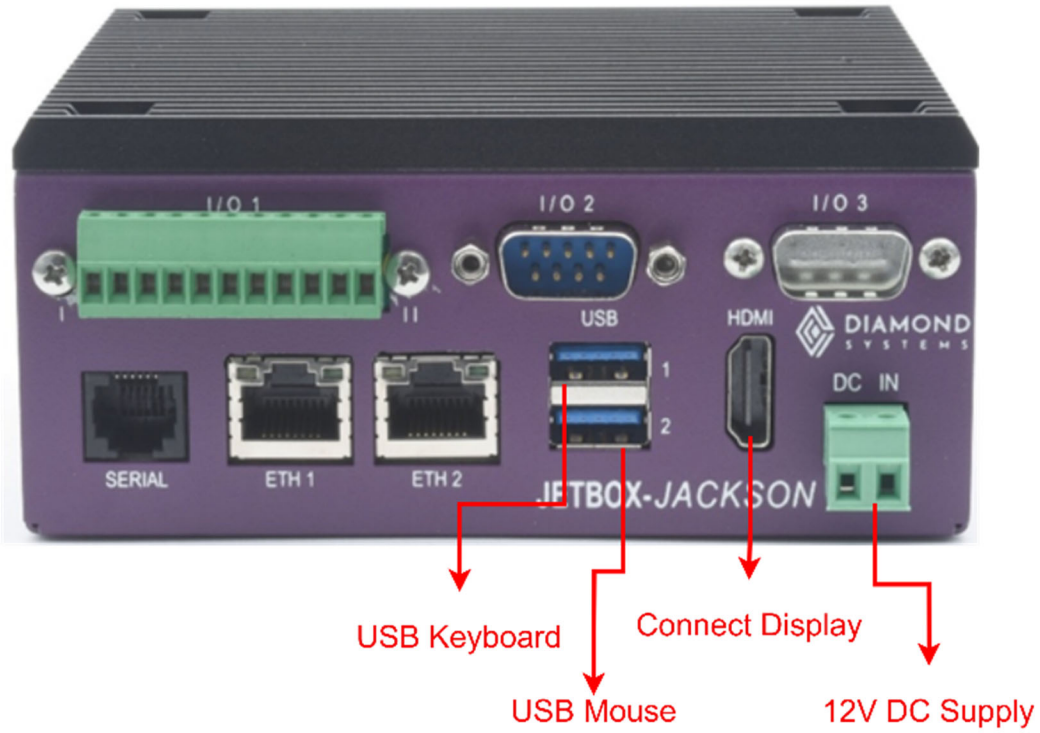


Figure 19-1: JetBox-Jackson Typical Set Up

Follow the steps provided below for JetBox-Jackson connections and boot to OS:

1. Connect the included 12V DC IN on front panel.
2. Connect the USB keyboard and mouse to USB ports 1 & 2 on the front panel.
3. Connect the HDMI monitor to HDMI port on the front panel.
4. Ensure that all the connections are intact.
5. Power ON the adapter and the module should now boot to OS.
6. On the Linux Welcome screen, fill in the basic details like Username, password, date & time.

The system boots into Ubuntu Desktop. Now, the system is set up and ready.

19.2. Flashing BSP Image

19.2.1. Format NVMe

Connect the NVMe drive to any host computer which has M.2 M-Key NVMe support.

Execute the command below to check the NVMe drive's device name:

```
lsblk -d -p | grep nvme
```

Execute the command below to create a new GPT:

```
sudo parted /dev/ mklabel gpt ex:
sudo parted /dev/nvme0n1 mklabel gpt
```

Execute the command below to add the APP partition:

```
sudo parted /dev/nvme0n1 mkpart APP 0GB 45GB
```

Execute the command below to format APP as an ext4 partition and mount it.

```
sudo mkfs.ext4 /dev/nvme0n1p1
```

19.2.2. Flash a Device

Connect M2M key device at J20 with proper format.

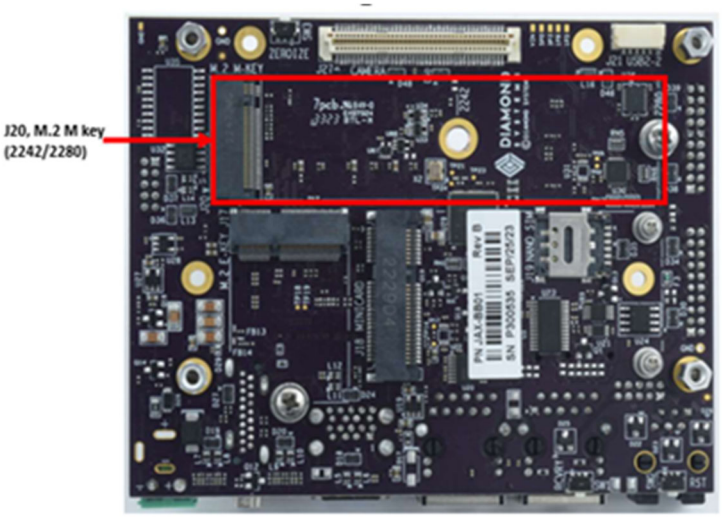


Figure 19-2: M2M Key Device at J20

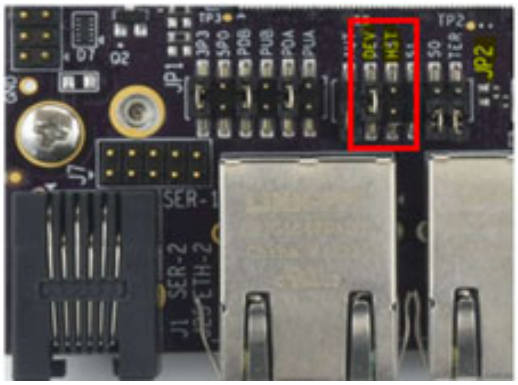


Figure 19-3: Insert into DEV

Remove the jumper from HST and insert it into DEV.

Power cycle the board by pressing and holding recovery SW button and release after 4 seconds. Connect USB A to USB A cable between J4 bottom port of Jackson board and Host PC installed with Ubuntu 20.4 x86_64, Kernel version: 5.15.0-52 or above.

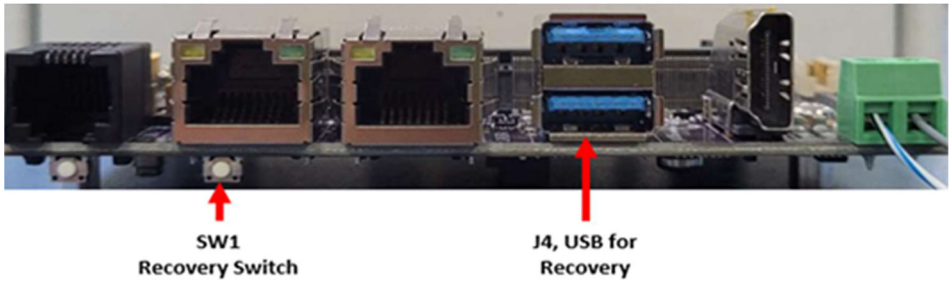


Figure 19-4: Connect USB cable

Open the Linux terminal in the Host PC and run 'lsusb' command to verify whether the board is in recovery mode or not. If board is booted in recovery mode, the Jetson Orin NX ™ will be detected as shown below.

```
hmecd001409@DSC:~$ lsusb
Bus 002 Device 001: ID 1d6b:0003 Linux Foundation 3.0 root hub
Bus 001 Device 035: ID 0955:7323 NVIDIA Corp. APX
Bus 001 Device 123: ID 413c:2107 Dell Computer Corp. Dell USB Entry Keyboard
Bus 001 Device 124: ID 413c:301a Dell Computer Corp. Dell MS116 USB Optical Mous
e
Bus 001 Device 001: ID 1d6b:0002 Linux Foundation 2.0 root hub
```

Figure 19-5: Verify board in recovery mode

Note: Similarly, the Jetson Orin Nano will be detected, but with different device ID. Refer below table for Orin NX and Orin Nano module's Device ID for different memory configuration.

7323	for Jetson Orin NX (P3767-0000 with 16 GB)
7423	for Jetson Orin NX (P3767-0001 with 8 GB)
7523	for Jetson Orin Nano (P3767-0003 and P3767-0005 with 8 GB)
7623	for Jetson Orin Nano (P3767-0004 with 4GB)

Run the following command to flash the Jackson package from your host machine to the carrier board.

```
sudo ./apply_binaries.sh

sudo ./tools/l4t_flash_prerequisites.sh
```

```
sudo ./tools/kernel_flash/l4t_initrd_flash.sh --external-device nvme0n1p1 -c
tools/kernel_flash/flash_l4t_external.xml -p "-c
bootloader/generic/cfg/flash_t234_qspi.xml" --showlogs --network usb0 jetson-orin-
nano-devkit internal
```

Figure 19-6: Module Reboots

The flashing process takes around 30 minutes to complete and below logs pop up upon completion.

When the flashing is complete, the module automatically reboots.

After rebooting, remove the USB cable at J4 bottom port and connect HDMI cable.

19.3. USB0 Host & Gadget Mode Configuration

To convert USB0 as host device, execute the commands below and reboot to apply changes.

Open the terminal and run the command ‘sudo otg_host’.

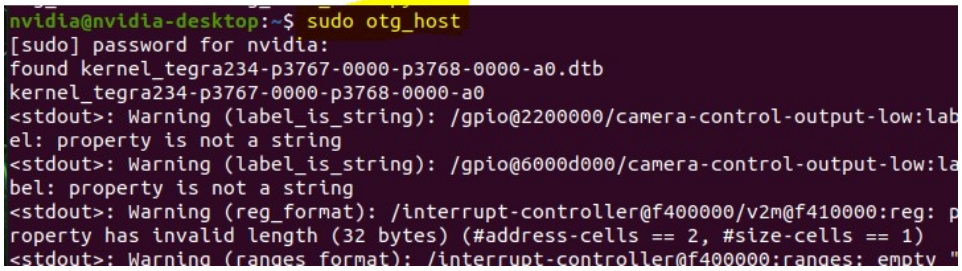


Figure 19-7: Run Command

Power off the board.

Remove DEV jumper and insert HST jumper on JP2.

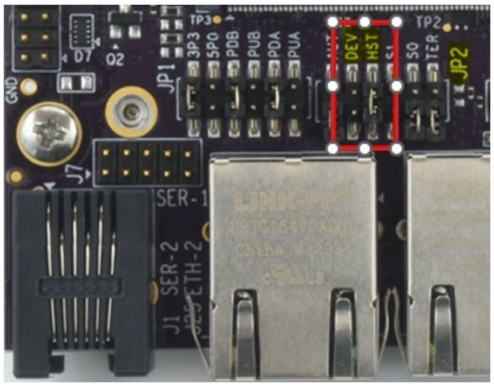


Figure 19-8: Insert HST Jumper

Connect the USB mouse to J4 bottom port and power on the board. Check whether the USB mouse is working.

20. Specifications

Features	
Jetson Module	Orin Nano or Orin NX
Cooling Accessory	Integrated heat spreader solution
Display	1x HDMI 2.0a/b
CAN Interface	1x CAN 2.0 Non-isolated transceiver standard, isolation optional consult factory (systems with Orin NX only)
Digital I/O	16x Digital IO obtained through I2C GPIO expander; see detailed specifications below
Ethernet	2x 10/100/1000 Mbps RJ45 with built-in magnetics and LEDs
Serial ports	1x RS-232 1x RS-232/485 (Configurable) (systems with Orin NX only)
USB Ports	2x USB 3.2
Utility	Force recovery and Reset buttons available on front panel
Digital I/O Specifications	
Device	PCA9535PW
Number of Lines	16
Direction	Programmable bit by bit
Logic Levels	3.3V/5V jumper configurable
Pull resistors	10K ohms +/-1%; Jumper-selectable pull-up/down
Input Voltage Thresholds	
Logic 0	-0.5V min, 0.99V(3.3V VIO), 1.5V(5V VIO) max
Logic 1	2.64V(3.3V VIO)/ 3.5V(5V VIO) min, 5.5V max
Output Voltage Thresholds	
Logic 0	0.0V min; 0.7V max @ 10mA output current
Logic 1	2.5V(3.3V VIO)/4V(5V VIO) min @ -10mA output current; 3.3V/5V max
Mechanical and Environmental Properties	
System Input Voltage	With Orin NX: 7-20VDC With Orin Nano: 5VDC +/-5%
Dimensions	124 W x 56 H x 99 D (mm) / 4.9 W x 2.2 H x 3.9 D (in)
Weight	0.698 kg. / 1.54 lbs.
Operating Temperature	-25°C to +80°C ambient (Est. 70C with Super Mode in full performance condition)
RoHS	Compliant